NPN
BDW42*
PNP
BDW46
BDW47*

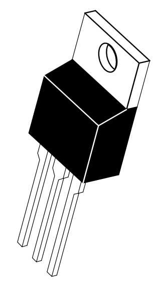
*Motorola Preferred Device

Darlington Complementary Silicon Power Transistors

. . . designed for general purpose and low speed switching applications.

- High DC Current Gain – h_{FE} = 2500 (typ.) @ I_C = 5.0 Adc.
- Collector Emitter Sustaining Voltage @ 30 mAdc:
  $V_{CEO(sus)}$ = 80 Vdc (min.) — BDW46
  100 Vdc (min.) — BDW42/BDW47
- Low Collector Emitter Saturation Voltage
  $V_{CE(sat)}$ = 2.0 Vdc (max.) @ I_C = 5.0 Adc
  3.0 Vdc (max.) @ I_C = 10.0 Adc
- Monolithic Construction with Built–In Base Emitter Shunt resistors
- TO–220AB Compact Package

DARLINGTON
15 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80 – 100 VOLTS
85 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BDW46	BDW42 BDW47	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous	I_C	15		Adc
Base Current	I_B	0.5		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	85 0.68		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.47	°C/W

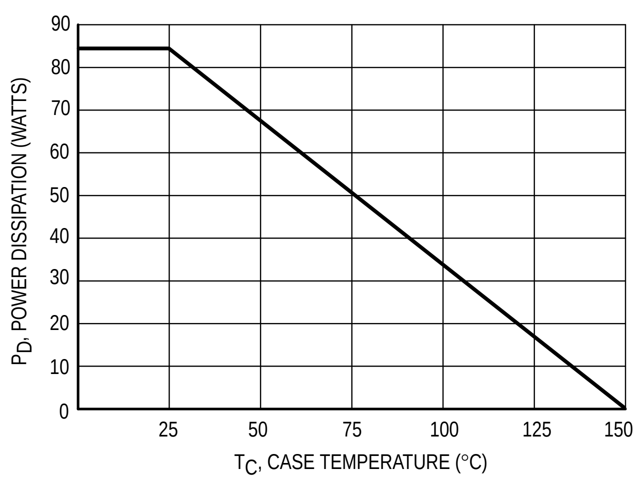


Figure 1. Power Temperature Derating Curve

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 7

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	 BDW46 BDW42/BDW47	$V_{CEO(sus)}$	 80 100	 — —	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 BDW46 BDW42/BDW47	I_{CEO}	 — —	 2.0 2.0	mAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	 BDW41/BDW46 BDW42/BDW47	I_{CBO}	 — —	 1.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)		h_{FE}	 1000 250	 — —	
Collector–Emitter Saturation Voltage (I_C = 5.0 Adc, I_B = 10 mAdc) (I_C = 10 Adc, I_B = 50 mAdc)		$V_{CE(sat)}$	 — —	 2.0 3.0	Vdc
Base–Emitter On Voltage (I_C = 10 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	—	3.0	Vdc
SECOND BREAKDOWN (2)					
Second Breakdown Collector Current with Base Forward Biased BDW42 BDW46/BDW47	 V_{CE} = 28.4 Vdc V_{CE} = 40 Vdc V_{CE} = 22.5 Vdc V_{CE} = 36 Vdc	$I_{S/b}$	 3.0 1.2 3.8 1.2	 — — — —	Adc
DYNAMIC CHARACTERISTICS					
Magnitude of common emitter small signal short circuit current transfer ratio (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		f_T	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	 BDW42 BDW46/BDW47	C_{ob}	 — —	 200 300	pF
Small–Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	—	

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2.0%.
(2) Pulse Test non repetitive: Pulse Width = 250 ms.

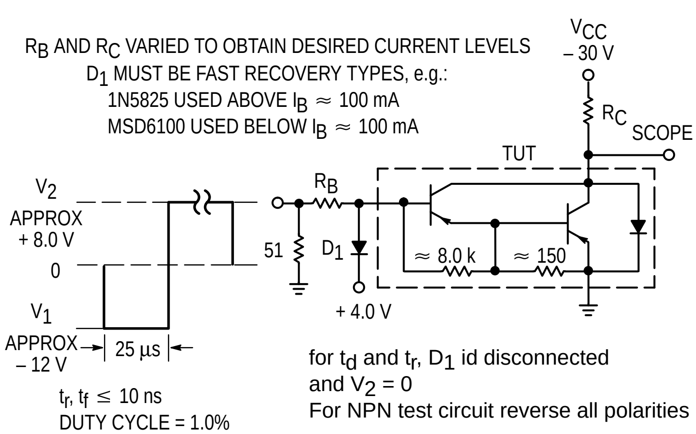


Figure 2. Switching Times Test Circuit

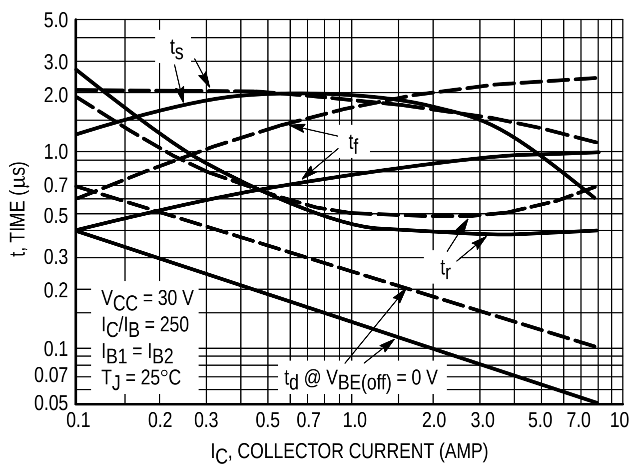


Figure 3. Switching Times

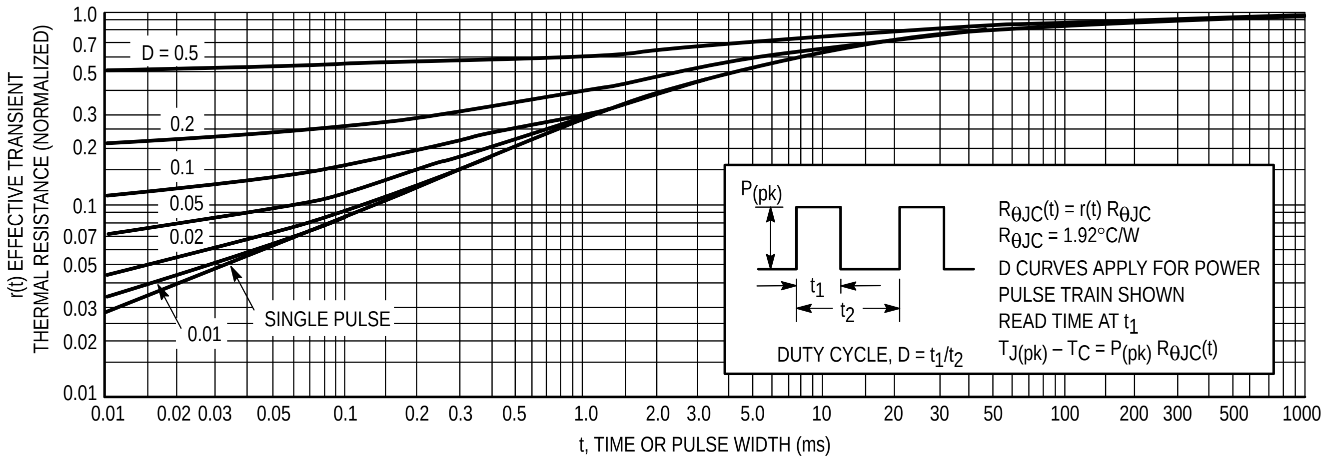


Figure 4. Thermal Response

ACTIVE–REGION SAFE OPERATING AREA

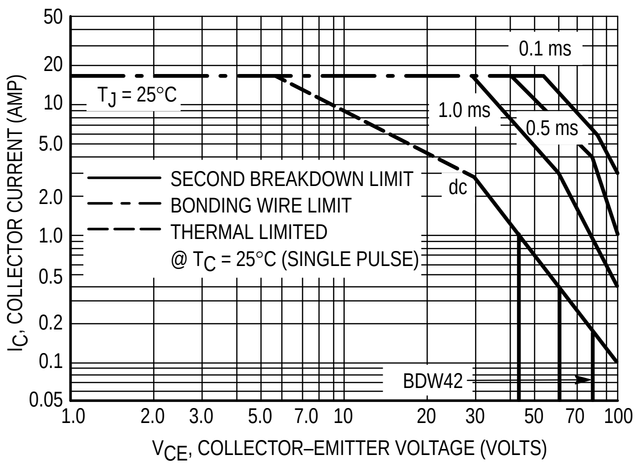


Figure 5. BDW42

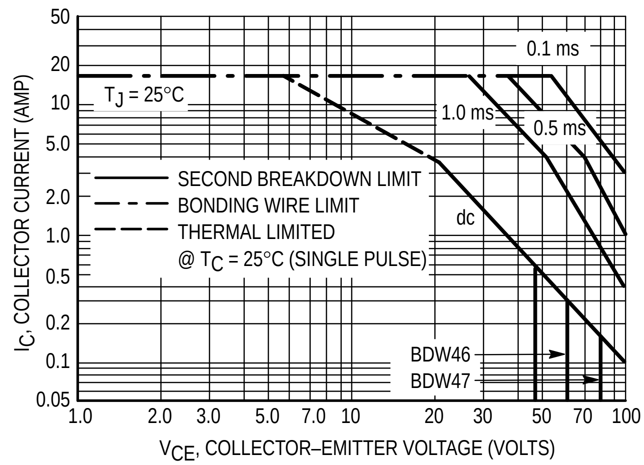


Figure 6. BDW46 and BDW47

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Fig. 5 and 6 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$. $T_{J(pk)}$ may be calculated from the data in Fig. 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

* Linear extrapolation

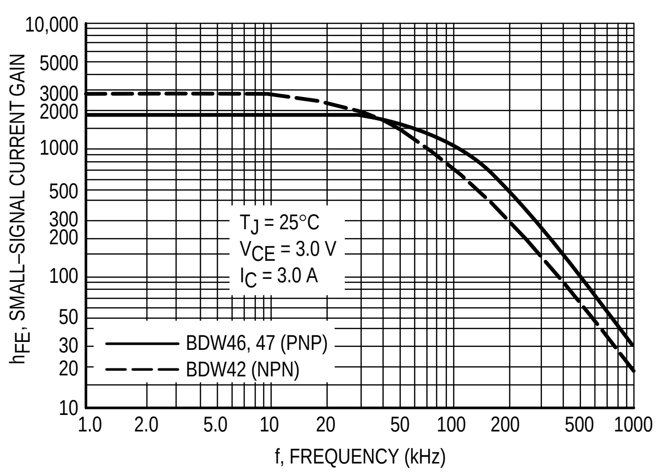


Figure 7. Small–Signal Current Gain

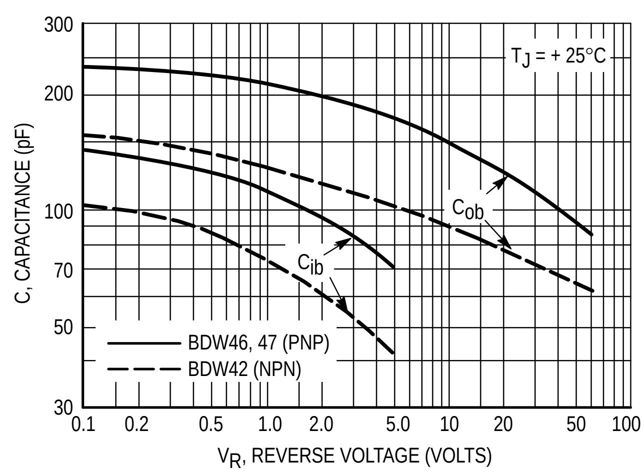
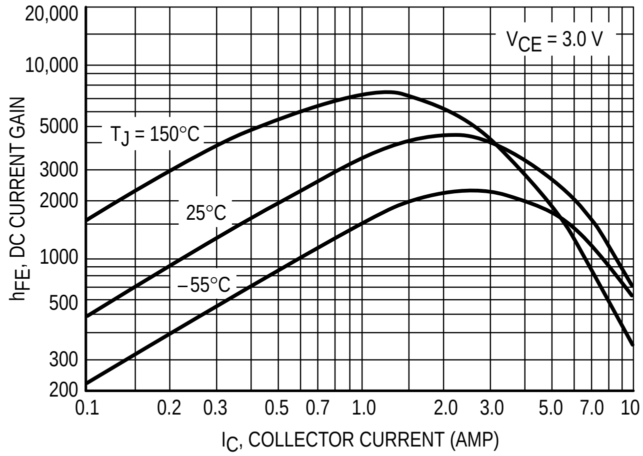


Figure 8. Capacitance

BDW40, 41, 42 (NPN)



BDW45, 46, 47 (PNP)

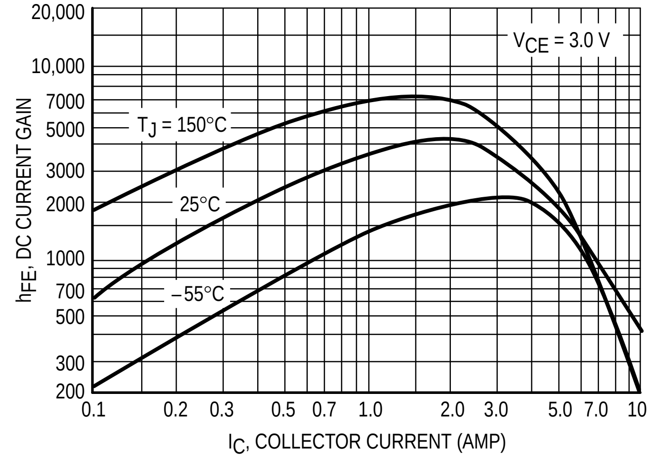
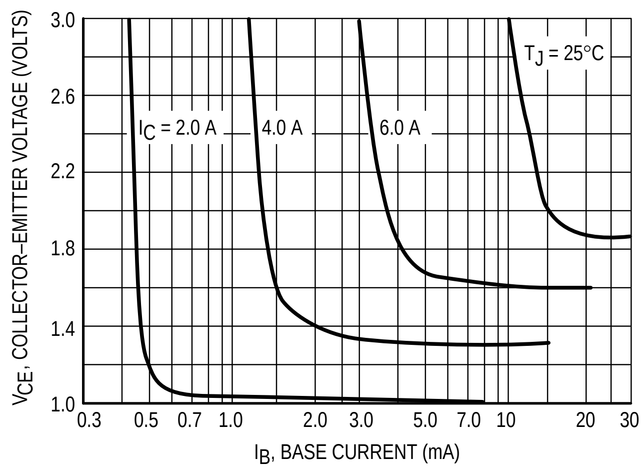


Figure 9. DC Current Gain



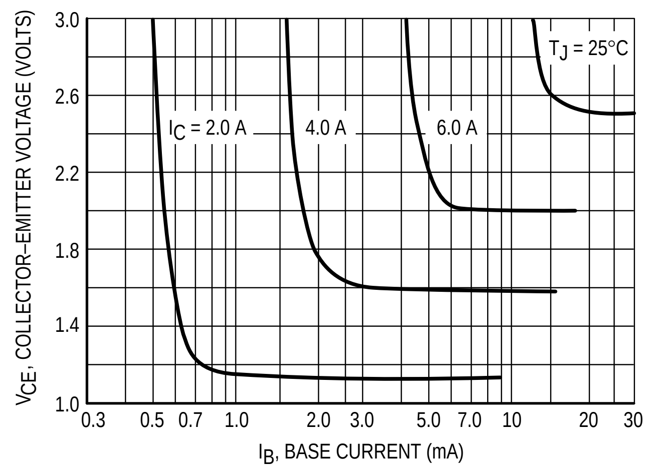
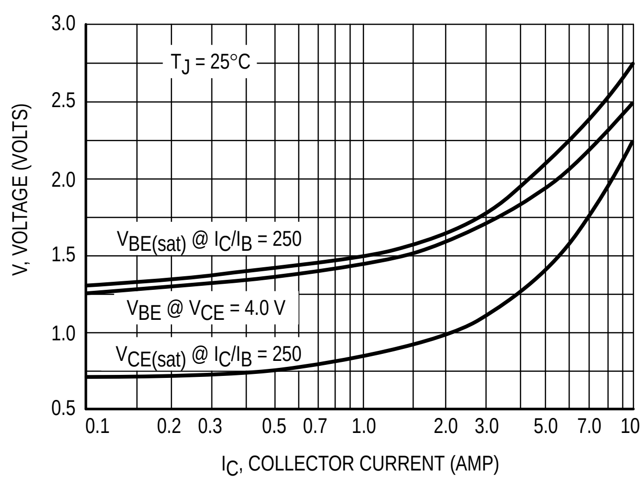


Figure 10. Collector Saturation Region

BDW40, 41, 42 (NPN)



BDW45, 46, 47 (PNP)

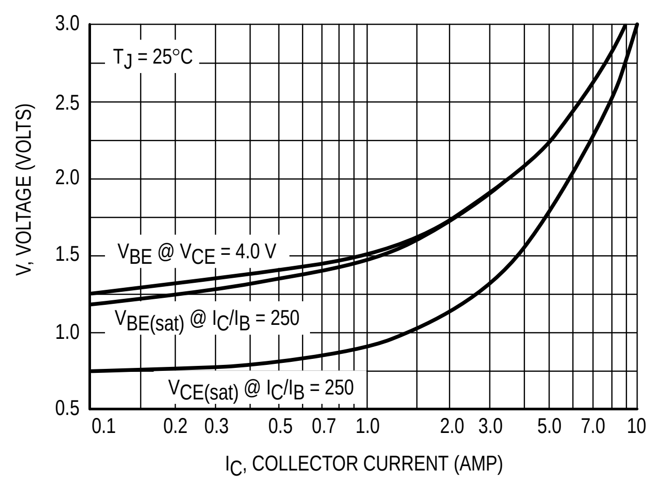


Figure 11. "On" Voltages

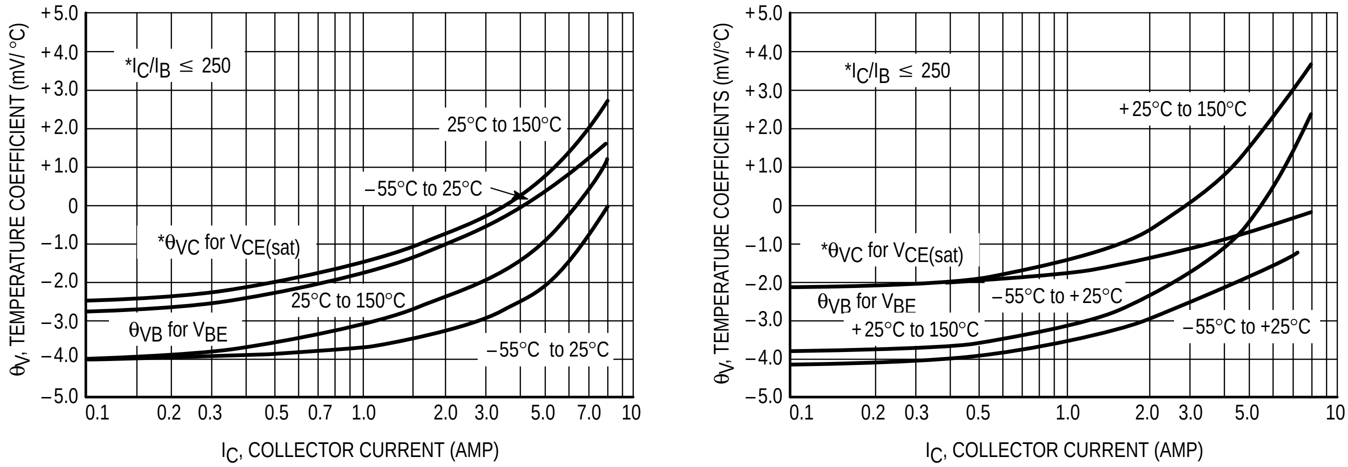


Figure 12. Temperature Coefficients

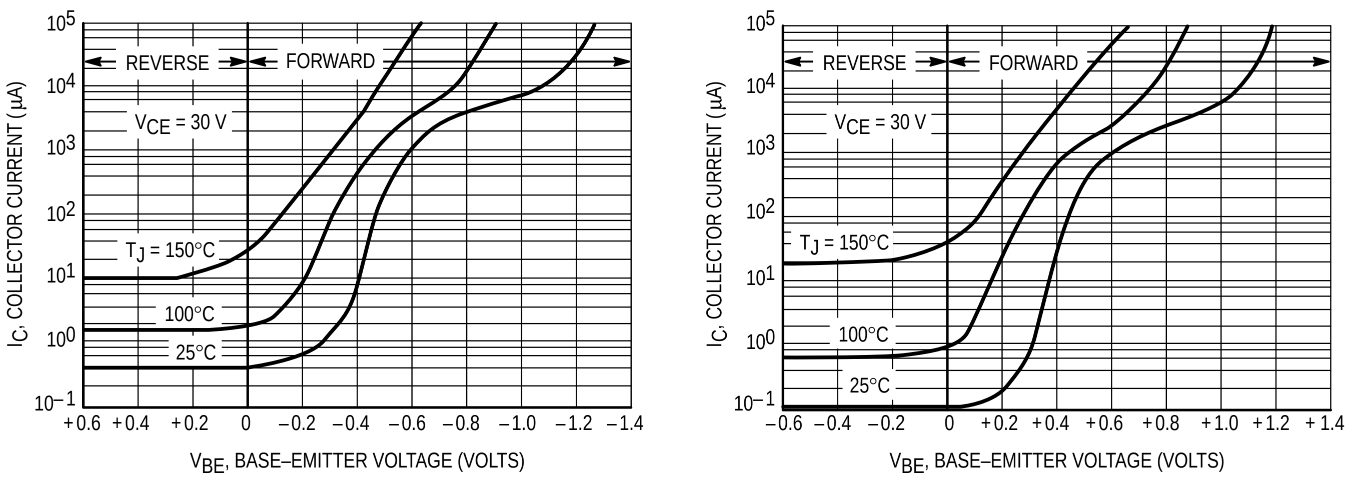
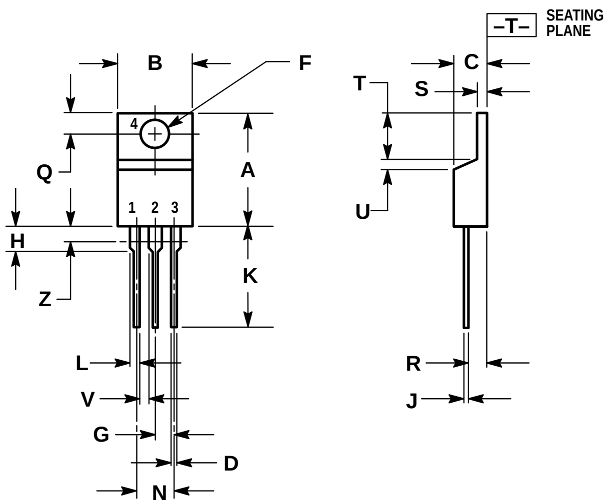


Figure 13. Collector Cut–Off Region

Figure 14. Darlington Schematic

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A–06
TO–220AB
ISSUE Y

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

MOTOROLA