GoldStar
## GOLD STAR CO., LTD.

GM76C28
CMOS 16K-BIT STATIC RAM

Description

The GM76C28 10/12 is a 2,048 words × 8 bits asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.
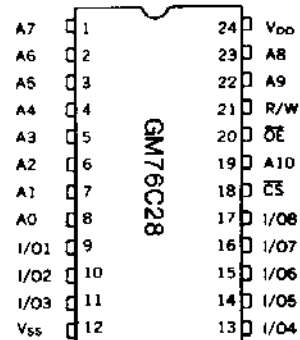
Features

- Access time ·· GM76C28-10 100ns (Max)
  GM76C28-12 120ns (Max)
- Low supply current ································· standby : 1μA (Typ)
  operation : GM76C28-10 30mA (Typ)
  GM76C28-12 25mA (Typ)
- Complete static operation
- Single power supply ······························· 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries

Schematic Diagram
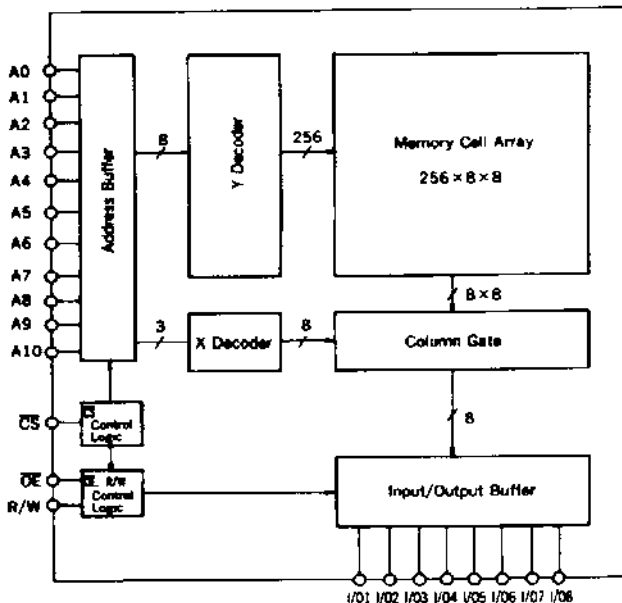
Pin Configuration

A0 to A10	Address Input
R/W	Read/Write
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O1 to 8	Data Input/Output
V_{DD}	Power Supply (+5V)
V_{SS}	Power Supply (0V)

Absolute Maximum Ratings

($V_{SS}=0V$)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Input voltage*	V_I	−0.5 to 7.0	V
Input/output voltage*	$V_{I/O}$	−0.5 to $V_{DD}+0.3$	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temp. & time	T_{sol}	260°C, 10s (at lead)	—

* V_I, $V_{I/O}$ = −1.0V when pulse width is 50 ns

Recommended Operating Conditions

(Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
	V_{SS}		0	0	0	V
Input voltage	V_{IH}		2.2	3.5	$V_{DD}+0.3$	V
	V_{IL}		−0.3*	—	0.8	V

* V_{IL}(Min)= −1.0V when pulse width is 50ns

Electrical Characteristics
DC Electrical Characteristics

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70°C)

Parameter	Symbol	Conditions	GM76C28-10 Min	GM76C28-10 Typ*	GM76C28-10 Max	GM76C28-12 Min	GM76C28-12 Typ*	GM76C28-12 Max	Unit
Input leakage current	I_{LI}	$V_{DD}=5.5V$, $V_I=0$ to V_{DD}	−1		1	−1	—	1	μA
Output leakage current	I_{LO}	$\overline{CS}=V_{IH}$, or $OE=V_{IH}$, $V_{I/O}=0$ to V_{DD}	−1		1	−1		1	μA
Operating supply current	I_{DDO}	$\overline{CS}=V_{IL}$, $I_{I/O}=0mA$	—	30	60		25	50	mA
	I_{DDO1}	$V_{IH}=3.5V$, $V_{IL}=0.6V$, $I_{I/O}=0mA$		16			16	--	mA
Average operating current	I_{DDA}	Min. cycle, duty=100%, $I_{I/O}=0mA$		30	60	—	25	50	mA
Standby supply current	I_{DDS}	$\overline{CS}=V_{IH}$		1.5	3.0		1.5	3.0	mA
	I_{DDS1}	$\overline{CS}=V_{DD}-0.2V$		1	50	--	1	50	μA
Output voltage	V_{OL}	$I_{OL}=4.0mA$	--	--	0.4	—	—	0.4	V
	V_{OH}	$I_{OH}=-1.0mA$	2.4	—	—	2.4	—	—	V

* Typical values are for reference, with $V_{DD}=5V$ and Ta=25°C assumed

Terminal Capacitance

(f = 1MHz, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_I	$V_I=0V$		4	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}=0V$	-	6	8	pF

AC Electrical Characteristics
Read Cycle

($V_{DD}=5V\pm10\%$, $V_{SS}=0V$, Ta=0 to 70°C)

Parameter	Symbol	Conditions	GM76C28-10 Min	GM76C28-10 Max	GM76C28-12 Min	GM76C28-12 Max	Unit
Read cycle time	t_{RC}		100	--	120		ns
Address access time	t_{ACC}	*1	—	100		120	ns
$\overline{CS}$ access time	t_{ACS}			100		120	ns
$\overline{CS}$ output setup time	t_{CLZ}	*2	10	—	10		ns
OE access time	t_{OE}	*1		55		60	ns
OE output setup time	t_{OLZ}		5		10		ns
$\overline{CS}$ output floating	t_{CHZ}	*2	0	40	0	40	ns
OE output floating	t_{OHZ}		0	40	0	40	ns
Output hold time	t_{OH}	*1	10		10		ns

Write Cycle

$(V_{DD}=5V\pm10\%, \ V_{SS}=0V, \ Ta=0 \text{ to } 70°C)$

Parameter	Symbol	Conditions	GM76C28-10		GM76C28-12		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	100	—	120	—	ns
Chip select time ($\overline{CS}$)	t_{CW}		80		85		ns
Address enable time	t_{AW}		80	—	85		ns
Address setup time	t_{AS}		0		0	—	ns
Write pulse width	t_{WP}		65	—	70	—	ns
$\overline{OE}$ output floating	t_{OHZ}	*2	0	40	0	40	ns
R/W output floating	t_{WHZ}	*3	0	45	0	50	ns
Input data setup time	t_{DW}		45	—	50		ns
Address hold time	t_{WR}	*1	5		5	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
R/W output setup time	t_{OW}	*3	5		10		ns

*1 Test conditions.
  1. Input pulse level: 0.8V to 2.2V
  2. tr = tf = 10ns
  3. Input/output timing reference level: 1.5V
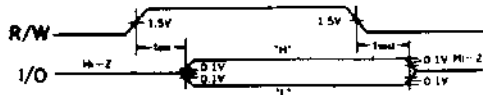 4. Output load: I_{OL} + C_L = 100pF

*3 Test conditions.
  1. Input pulse level: 0.8V to 2.2V
  2. tr = tf = 10ns
  3. Test circuit

*2 Test conditions.
  1. Input pulse level: 0.8V to 2.2V
  2. tr = tf = 10ns
  3. Test circuit

o Both SW1 and SW2 are closed when measuring t_{CHZ} or t_{OHZ}.
o SW1 is open and SW2 is closed when measuring Hi-z-high of t_{OLZ} or t_{CLZ}.
o SW1 is closed and SW2 is open when measuring Hi-z-low of t_{OLZ} or t_{CLZ}.

Output turnon turnoff times

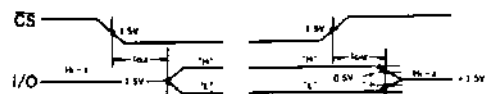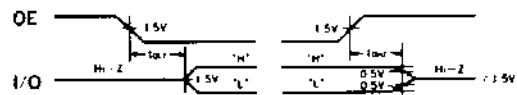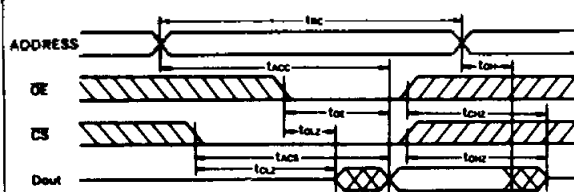o SW is set to the V_{DD} side when measuring Hi-z-high and high-Hi-z of t_{OW} or t_{WHZ}.
o SW is set to the V_{SS} side when measuring Hi-z-low and low-Hi-z of t_{OW} or t_{WHZ}.

Output turnon turnoff times

Timing Chart

o Read cycle 1 ($\overline{OE}$, $\overline{CS}$ control, R/W = high)

o Read cycle 2 (R/W control, $\overline{OE}$ = low, $\overline{CS}$ = low)

○ Write cycle 1 (R/W control, OE = low)

○ Write cycle 2 (R/W control)

○ Write cycle 3 (CS control, OE = low)
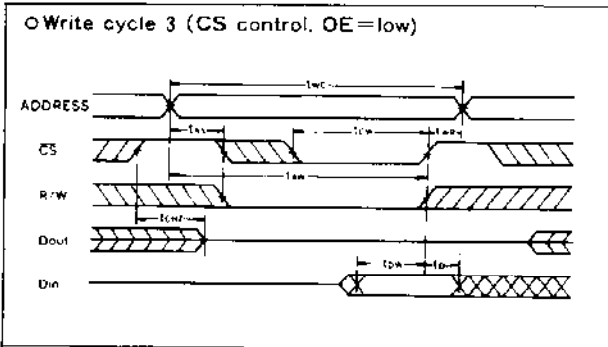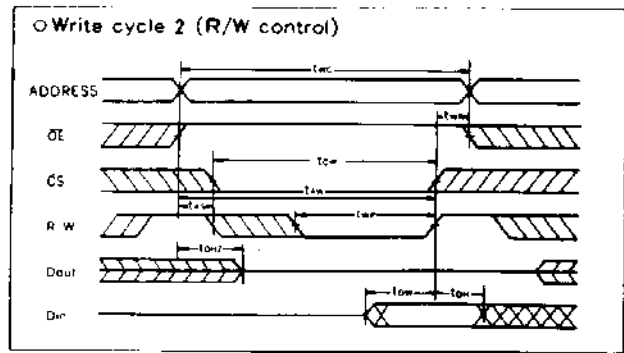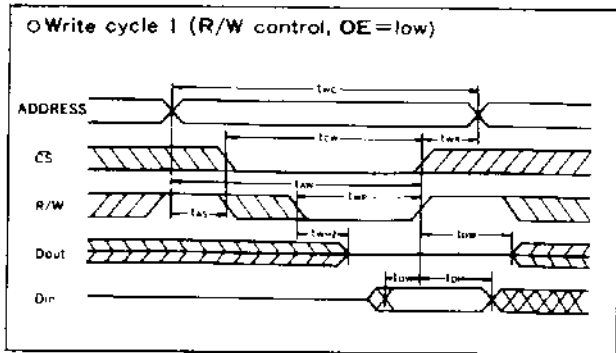
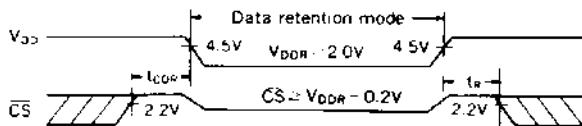## Data Retention Characteristics with Low Voltage Power Supply

(Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDR}	$\overline{CS} \geq V_{DDR} - 0.2V$	2.0	—	5.5	V
Data retention current	I_{DDR}	$V_{DD} = 3.0V$, $\overline{CS} \geq 2.8V$	—	—	25	μA
Chip select data hold time	t_{CDR}	Refer to the figure below.	0	—	—	ns
Operation recovery time	t_R		t_{RC} *	—	—	ns

* t_{RC} : read cycle time

Data retention timing

Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

Functions

Truth Table

$\overline{CS}$	$\overline{OE}$	R/W	A0 to A10	DATA I/O	Mode	I_{DD}
H			—	Hi-Z	Unselected	I_{DDS}, I_{DDS1}
L	L	H	Stable	Output data	Read	I_{DDO}
L	H	L	Stable	Input data	Write	I_{DDO}
L	L	L	Stable	Input data	Write	I_{DDO}

X : "H" or "L", — : "H", "L" or "Hi-Z"

Reading Data

Data can be read out if an address is set while $\overline{CS}$ and $\overline{OE}$ are held low, and R/W is held high.

Writing Data

There are following three ways of writing data.

(1) Hold $\overline{CS}$ low, set the address, and apply a low pulse to R/W.

(2) Hold R/W low, set the address, and apply a low pulse to $\overline{CS}$.

(3) Set the address, then apply low pulses to both $\overline{CS}$ and R/W.

In any case, data from the DATA I/O terminal is fetched into the GM76C28$_{10/12}$ at the last transition of a section in which both $\overline{CS}$ and R/W are low. Because the DATA I/O terminal is in high-impedance state when $\overline{CS}$ or $\overline{OE}$ is high, or R/W is low, contention of data driver on the bus and memory output is avoided.

Standby Mode

When $\overline{CS}$ is high, GM76C28 is in standby mode and only retains the data. At this time the DATA I/O terminal is in high-impedance state and input of an address, R/W signal, or data is prohibited. When $\overline{CS}$ is above $V_{DD} - 0.2V$, current flow within the GM76C28 chip is only that in the high-resistance portion of memory cells and leakage current.

Characteristics Curves

Plot titles, left to right, top to bottom:

I_{DDO}—Ta $V_{DD} = 5.5V$, $\overline{CS} = 0.8V$

I_{DDO}—V_{DD} $Ta = 25°C$, $\overline{CS} = 0.8V$

I_{DDA}—t_{cyc} $V_{DD} = 5.5V$, $Ta = 25°C$

I_{DDS1}—Ta $V_{DD} = 5.5V$, $\overline{CS} \geq V_{DD} - 0.2V$

I_{DDS1}—V_{DD} $Ta = 25°C$, $\overline{CS} > V_{DD} - 0.2V$

I_{OH}—V_{OH} $V_{DD} = 4.5V$, $Ta = 25°C$

Normalized $t_{ACC} \cdot t_{ACS} \cdot t_{OE}$—Ta $V_{DD} = 4.5V$, $C_L = 100pF$

Normalized $t_{ACC} \cdot t_{ACS} \cdot t_{OE}$—$V_{DD}$ $Ta = 25°C$, $C_L = 100pF$

I_{OL}—V_{OL} $V_{DD} = 4.5V$, $Ta = 25°C$