2

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C)

Function	Type ①		Loading Factor Each Output	Propagation Delay ns typ	Power Dissipation mW typ/pkg	Case
	-55 to +125°C	0 to +75°C				
Quad 2-Input Gate, 4 NOR Outputs w/o Pulldowns	MC1212F,L	MC1012P	25	4.5	65	607, 632, 646
AC Coupled J-K Flip-Flop (85 MHz typ)	MC1213F,L	MC1013P	25	6.0	125	607, 632, 646
Dual R-S Flip Flop (Positive Clock)	MC1214F,L	MC1014P	25	6.0	140	607, 632, 646
Dual R-S Flip-Flop (Negative Clock)	MC1215F,L	MC1015P	25	6.0	140	607, 632, 646
Dual R-S Flip-Flop (Single Rail)	MC1216F,L	MC1016P	25	6.0	140	607, 632, 646
Level Translator (Saturated Logic to MECL)	MC1217F,L	MC1017P	25 (MECL)	15	105	607, 632, 646
Level Translator (MECL to Saturated Logic)	MC1218F,L	MC1018P	7 (DTL)	19	55	607, 632, 646
Full Adder	MC1219F,L	MC1019P	25	3.0 to 8.0**	145	607, 632, 646
Quad Line Receiver	MC1220F,L	MC1020P	25	4.0	115	607, 632, 646
Full Subtractor	MC1221F,L	MC1021P	25	4.0 to 11**	145	607, 632, 646
Type D Flip-Flop	MC1222F,L	MC1022P	25	8.0	110	607, 632, 646
Dual 4-Input OR/NOR Clock Driver *	MC1223F,L	MC1023P	25	2.0	250	607, 632, 646
Dual 2-Input Expandable Gate	MC1224L	MC1024P	25	4.0	95	632, 646
Dual 4 and 5-Input Expander	MC1225F,L	MC1025P		-	-	607, 632, 646
Dual 3-4-Input Transmission Line and Clock Driver *	MC1226F,L	MC1026P	25	2.0	140	607, 632, 646
AC Coupled J K Flip-Flop (120 MHz typ)	MC1227F,L	MC1027P	25	4.0	250	607, 632, 646
Dual 4-Channel Data Selector *	MC1228F,L	MC1028P	25	5.0	170	620, 648, 650
Quad Exclusive OR Gate	MC1230F,L	MC1030P	25	5.0	130	607, 632, 646
Quad Exclusive NOR Gate	MC1231F,L	MC1031P	25	5.0	130	607, 632, 646
100-MHz AC Coupled Dual J K Flip Flop *	MC1232F,L	MC1032P	25	4.5	180	620, 648, 650
Dual R-S Flip-Flop (Single Rail, Negative Clock)	MC1233F,L	MC1033P	25	6.0	140	607, 632, 646
Type D Flip-Flop *	MC1234F,L	MC1034P	25	4.0	185	607, 632, 646
Triple Line Receiver	MC1235F,L	MC1035P	25	5.0	140	607, 632, 646
16-Bit Coincident Memory *	MC1236F,L	MC1036P	5	17	250	607, 632, 646
16 Bit Coincident Memory w/o Pulldowns *	MC1237F,L	MC1037P	5	17	250	607, 632, 646
Quad Level Translator (MECL to Saturated Logic)	MC1239F,L	MC1039P	7 (DTL)	12	200	620, 648, 650
Quad Latch	MC1240F,L	MC1040P	25	8.0	250	607, 632, 646
Decoder - Display Driver *	MC1245F,L	MC1045P		-	178	620, 648, 650
Quad 2 Input AND Gates	MC1247F,L	MC1047P	25	5.0	130	607, 632, 646
Quad 2-Input NAND Gates	MC1248F,L	MC1048P	25	5.0	130	607, 632, 646
Dual Full Adder *	MC1259F,L	MC1059P	25	9.0	375	620, 648, 650
Quad 2-Input NOR Gate *	MC1262F,L	MC1062P	25	2.0	320	620, 648, 650
Quad 2-Input NOR Gate *	MC1263L	MC1063P	25	2.0	320	632, 646
Triple Line Receiver *	MC1266F,L	MC1066P	26	2.0	350	607, 632, 646
Quad MTTL to MECL Translator With Strobe	MC1267F,L	MC1067P	1	5.0	300	620, 648, 650
Quad MECL to MTTL Translator With Totem-Pole Outputs *	MC1268F,L	MC1068P	10 (MTTL)	5.0	340	620, 648, 650
Quad Latch	MC1270F,L	MC1070P	25	8.0	200	607, 632, 646

① Type numbers with F suffix use Case 607 or 650, Type numbers with L suffix use Case 632 or 620 as indicated.
Type numbers with P suffix use Case 646 or 648 as indicated.

† Not recommended for new designs

*Noise Margin = 150 mV

**Propagation delay time is dependent on data path, see data sheet for details.