Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TBB 202	Q67000-H8217	P-DIP-8
TBB 202 G	Q67000-H8218	P-DSO-8 (SMD)

The TBB 202 is specially intended for applications in radiotelephones. It contains several ECL divider stages, which have a total divider ratio of 1:128/129, depending on the control of the MOD input. It can be employed in standby-mode (input STB = Low).

Circuit Description

The divider has balanced push-pull inputs. If it is driven unbalanced, the unused input has to be blocked by a capacitor (approx. 1.5 nF) with low series inductance. The divider of the component consists of several status-controlled master-slave flipflops, which have a total divider ratio of 1:128/129. The inputs MOD (divider ratio) and STB (standby mode) are controllable with TTL levels. The ECL output of the divider is compatible with all standard PLL circuits. The typical swing is 1 V_{PP}. **No load resistance is required.**

Truth Table for Operating Modes

Input	Level	Function
MOD	HIGH or unwired LOW	1:128 1:129
STB	HIGH or unwired LOW	NORMAL HIGH, STANDBY

Preliminary Data **Bipolar IC**

Type	Ordering Code	Package
TBB 212	Q67000-H8204	P-DIP-8
TBB 212 G	Q67000-H8205	P-DSO-8 (SMD)

The TBB 202 is specially intended for applications in radiotelephones. It contains several ECL divider stages, which have a total divider ratio of 1:64/65, depending on the control of the MOD input. It can be employed in standby-mode (input STB = Low). The IC is particular intended for GSM.

Circuit Description

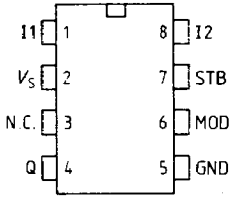
The divider has balanced push-pull inputs. It is driven unbalanced, the unused input has to be blocked by a capacitor (approx. 1.5 nF) with low series inductance. The divider of the component consists of several status-controlled master/slave flipflops, which have a total divider ratio of 1:64/65. The MOD inputs (divider ratio changeover input) and STB (input for standby mode) are controllable with TTL levels. The ECL output of the divider is compatible with all standard PLL circuits. The typical swing is 1 V_{PP} no load resistance is required.

Truth Table for Operating Modes

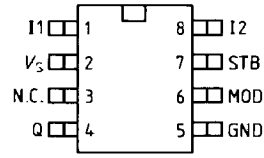
Input	Level	Function
MOD	HIGH or unwired LOW	1:64 1:65
STB	HIGH or unwired LOW	NORMAL HIGH, STANDBY

Pin Configurations
(top view)

TBB 202, TBB 212



TBB 202 G, TBB 212 G



Pin Description

Pin No.	Symbol	Function
1	I1	Input
2	V_S	Supply voltage
3	N.C.	not connected
4	Q	Output
5	GND	Ground
6	MOD	Input for control of divider ratio
7	STB	Input for standby mode
8	I2	Input

Absolute Maximum Ratings

$T_A = -40\,°C$ to $85\,°C$

Parameter	Symbol	Values min.	Values max.	Unit
Supply voltage	V_S	−0.3	6	V
Input voltage (pin 1; pin 8)	V_I	−0.3	2.5	V
Input voltage (pin 6; pin 7)	$V_{MOD}V_{STB}$	−0.3	6	V
Output voltage (pin 4)	V_Q		V_S	V
Output current (pin 4)	$-I_Q$		10	mA
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−65	125	°C
Thermal resistance				
system – air P-DIP-8	$R_{th\,SA}$		105	K/W
P-DSO-8	$R_{th\,SA}$		180	K/W

Operating Range

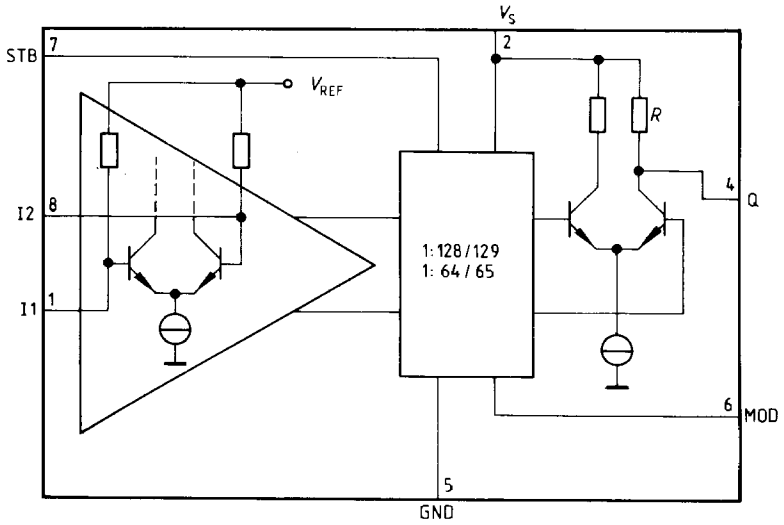
Supply voltage	V_S	3.0	5.5	V
Input frequency	f	200	1100	MHz
Ambient temperature	T_A	−40	85	°C

Characteristics

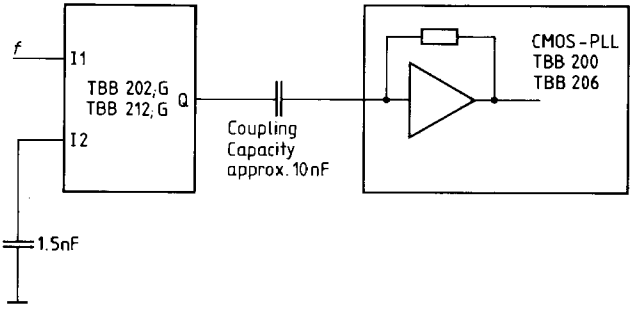
V_S = 3.0 V to 5.5 V, T_A = −40 °C to 85 °C

Parameter	Symbol	Values min.	Values typ.	Values max.	Unit	Test Conditions	Test Circuit
Current consumption in operation						Inputs blocked STB open, no load T_A = 25 °C	1
	I_S		8		mA	V_S = 3 V	
	I_S		9		mA	V_S = 4 V	
	I_S		9.5		mA	V_S = 5 V	
in standby						Output n.c. STB = GND	
	I_S		1.5		mA	Inputs blocked	1
Input level (input sensitivity)	V_I					Output n.c., STB = V_S	
		10		100	mV_{rms}	200 MHz (sine voltage)	1
		5		100	mV_{rms}	400 MHz	1
		5		100	mV_{rms}	600 MHz	1
		5		100	mV_{rms}	800 MHz	1
		7		100	mV_{rms}	900 MHz	1
		10		100	mV_{rms}	1000 MHz	1
MOD Input							
Switching threshold	V_I		0.7		V		1
H-input current	I_{IH}		0	50	µA	MOD = V_S	1
L-input current	$-I_L$		110	200	µA	MOD = ground	1
Standby Input							
Switching threshold	V_{STB}		0.7		V		
H-input current	I_{IH}			50	µA	STB = V_S	1
L-input current	$-I_{IL}$			200	µA	STB = ground	1
Output							
Output voltage swing	V_Q		1		V_{pp}	$C_L \leq 15$ pF	1
Output resistance	R		1		kΩ		
Switching Times							
Setup time	$t_{Setup\,1}$, $t_{Setup\,2}$		5		ns		
Hold time	$t_{Hold\,1}$, $t_{Hold\,2}$		5		ns		

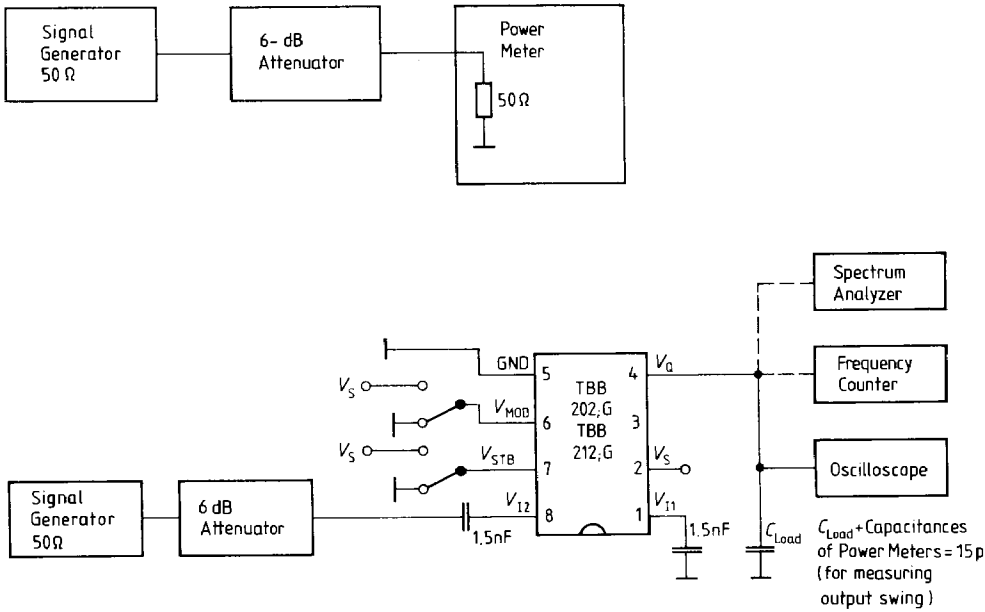
Block Diagram



Application Circuit



Test Circuit 1



Diagram