2101A/8101A-4*

256 X 4 BIT STATIC RAM

2101A-2	250 ns Max.
2101A	350 ns Max.
2101A-4	450 ns Max.

- 256 x 4 Organization to Meet Needs for Small System Memories
- Single +5V Supply Voltage
- Directly TTL Compatible: All Inputs and Output
- Statis MOS: No Clocks or Refreshing Required
- Simple Memory Expansion: Chip Enable Input
- Inputs Protected: All Inputs Have Protection Against Static Charge
- Low Cost Packaging: 22 Pin Plastic Dual In-Line Configuration
- Low Power: Typically 150 mW
- Three-State Output: OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

The Intel® 2101A is a 256 word by 4-bit static random access memory element using N-channel MOS devices integrated on a monolithic array. It uses fully DC stable (static) circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data.

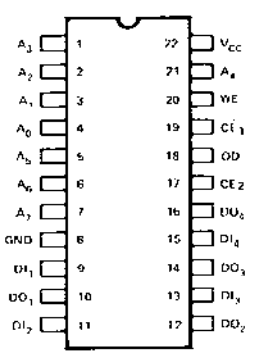
The 2101A is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bi-directional logic in a common I/O system.

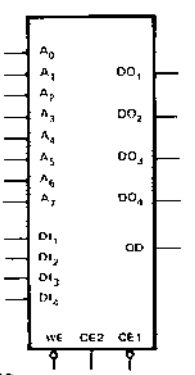
The Intel® 2101A is fabricated with N-channel silicon gate technology. This technology allows the design and production of high performance, easy-to-use MOS circuits and provides a higher functional density on a monolithic chip than either conventional MOS technology or P-channel silicon gate technology.

Intel's silicon gate technology also provides excellent protection against contamination. This permits the use of low cost plastic packaging.

PIN CONFIGURATION



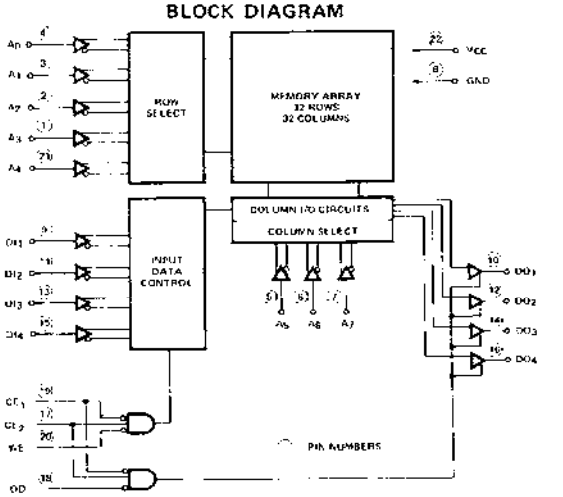
LOGIC SYMBOL



PIN NAMES

DI_1, DI_4	DATA INPUT	$\overline{CE}_2$	CHIP ENABLE 2
A_0 A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
$\overline{WE}$	WRITE ENABLE	DO_1, DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

BLOCK DIAGRAM



*All 8101A-4 specs are identical to the 2101A-4 specs.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . -10°C to 80°C

Storage Temperature . . . . . -65°C to +150°C

Voltage On Any Pin
With Respect to Ground . . . . . 0.5V to +7V

Power Dissipation . . . . . 1 Watt

*COMMENT:

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

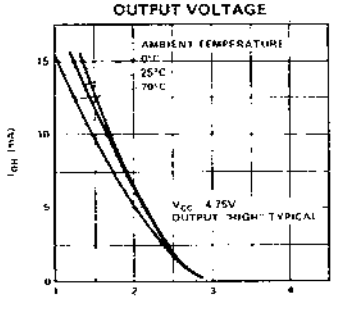
D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

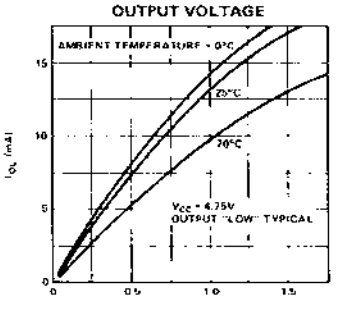
Symbol	Parameter		Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	Data Output Leakage Current			1	10	µA	Output Disabled, V_{OUT}=4.0V
I_{LOL}	Data Output Leakage Current			-1	-10	µA	Output Disabled, V_{OUT}=0.45V
I_{CC1}	Power Supply Current	2101A, 2101A-4		35	55	mA	V_{IN} = 5.25V, I_O = 0mA
		2101A-2		45	65		T_A = 25°C
I_{CC2}	Power Supply Current	2101A, 2101A-4			60	mA	V_{IN} = 5.25V, I_O = 0mA
		2101A-2			70		T_A = 0°C
V_{IL}	Input "Low" Voltage		-0.5		+0.8	V	
V_{IH}	Input "High" Voltage		2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage				+0.45	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2101A, 2101A-2	2.4			V	I_{OH} = -200µA
		2101A-4	2.4			V	I_{OH} = -150µA

TYPICAL D.C. CHARACTERISTICS

OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.

A.C. CHARACTERISTICS FOR 2101A-2 (250 ns ACCESS TIME)

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	
t_A	Access Time			250	ns	t_r, t_f = 20ns
t_{CO}	Chip Enable To Output			180	ns	Input Levels = 0.8V or 2.0V
t_{OD}	Output Disable To Output			130	ns	Timing Reference = 1.5V
t_{DF}[3]	Data Output to High Z State	0		180	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid after change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE

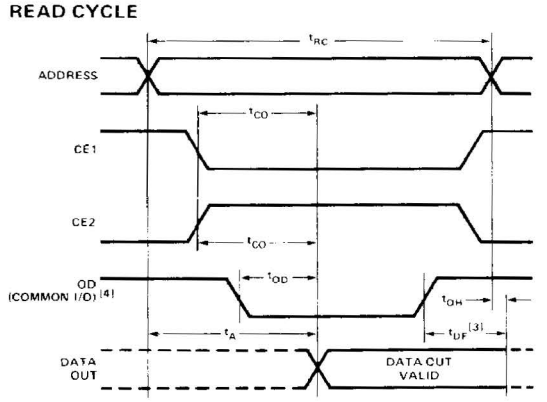
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	170			ns	
t_{AW}	Write Delay	20			ns	t_r, t_f = 20ns
t_{CW}	Chip Enable To Write	150			ns	Input Levels = 0.8V or 2.0V
t_{DW}	Data Setup	150			ns	Timing Reference = 1.5V
t_{DH}	Data Hold	0			ns	Load = 1 TTL Gate
t_{WP}	Write Pulse	150			ns	and C_L = 100pF.
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

CAPACITANCE[2] $T_A = 25°C$, f = 1MHz

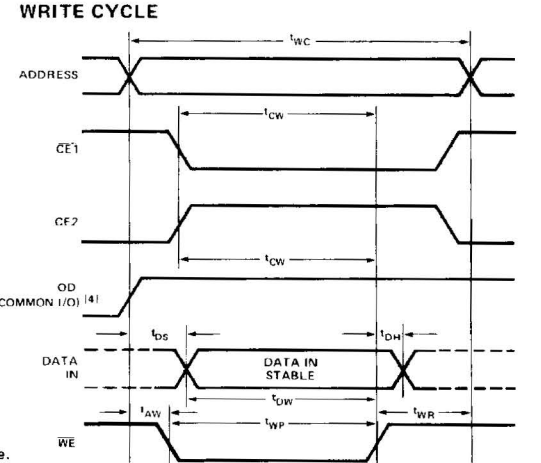
Symbol	Test	Limits (pF)	
		Typ.[1]	Max.
C_{IN}	Input Capacitance (All Input Pins) V_{IN} = 0V	4	8
C_{OUT}	Output Capacitance V_{OUT} = 0V	8	12

WAVEFORMS

READ CYCLE



WRITE CYCLE



NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.
4. OD should be tied low for separate I/O operation.

2101A (350 ns ACCESS TIME)

A.C. CHARACTERISTICS

READ CYCLE T_A = 0°C to 70°C, V_{CC} 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	
t_A	Access Time			350	ns	t_r, t_f = 20ns
t_{CO}	Chip Enable To Output			240	ns	Input Levels = 0.8V or 2.0V
t_{OD}	Output Disable To Output			180	ns	Timing Reference 1.5V
t_{DF} [2]	Data Output to High Z State	0		150	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid after change of Address	40			ns	and C_L 100pF.

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	220			ns	
t_{AW}	Write Delay	20			ns	t_r, t_f 20ns
t_{CW}	Chip Enable To Write	200			ns	Input Levels = 0.8V or 2.0V
t_{DW}	Data Setup	200			ns	Timing Reference 1.5V
t_{DH}	Data Hold	0			ns	Load = 1 TTL Gate
t_{WP}	Write Pulse	200			ns	and C_L 100pF.
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

2101A-4 (450 ns ACCESS TIME)

A.C. CHARACTERISTICS

READ CYCLE T_A = 0°C to 70°C, V_{CC} 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	450			ns	
t_A	Access Time			450	ns	t_r, t_f = 20ns
t_{CO}	Chip Enable To Output			310	ns	Input Levels = 0.8V or 2.0V
t_{OD}	Output Disable To Output			250	ns	Timing Reference = 1.5V
t_{DF} [2]	Data Output to High Z State	0		200	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid after change of Address	40			ns	and C_L 100pF.

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	270			ns	
t_{AW}	Write Delay	20			ns	t_r, t_f = 20ns
t_{CW}	Chip Enable To Write	250			ns	Input Levels = 0.8V or 2.0V
t_{DW}	Data Setup	250			ns	Timing Reference = 1.5V
t_{DH}	Data Hold	0			ns	Load = 1 TTL Gate
t_{WP}	Write Pulse	250			ns	and C_L = 100pF.
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

NOTES 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2, or $\overline{OD}$, whichever occurs first.