

7442, LS42 Decoders

BCD-To-Decimal Decoder (1-of-10)
Product Specification

FEATURES

- Mutually exclusive outputs
- 1-of-8 demultiplexing ability
- Outputs disabled for input codes above nine

DESCRIPTION

The '42 decoder accepts four active HIGH BCD inputs and provides 10 mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the '42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input, A_3 , produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
7442	15ns	28mA
74LS42	18ns	7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7442N, N74LS42N
Plastic SO	N74LS54D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

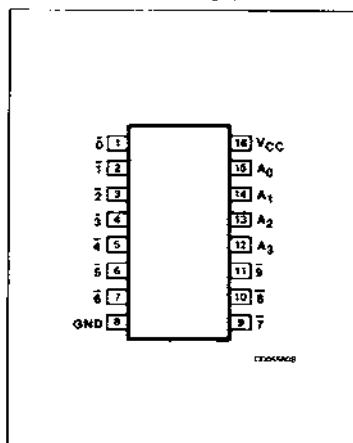
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
$A_0 - A_3$	Inputs	1uI	1LSuI
$\bar{0} - \bar{9}$	Outputs	10uI	10LSuI

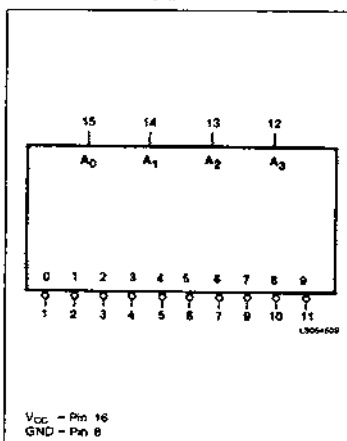
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} and a 74LS unit load (LSuI) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

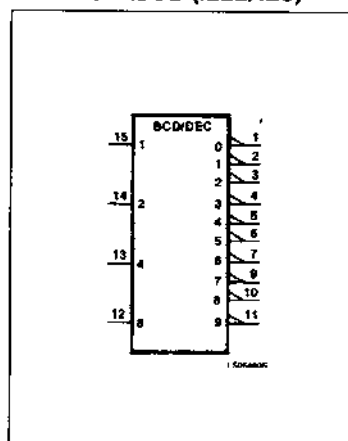
PIN CONFIGURATION



LOGIC SYMBOL



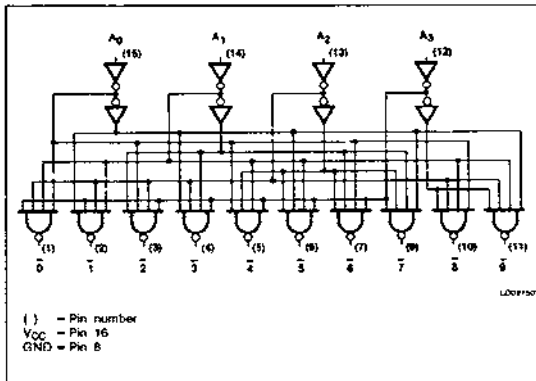
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



FUNCTION TABLE

A_3	A_2	A_1	A_0	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	H	H	H	H	H	H	H	L	H	H	H
H	L	L	L	H	H	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
 L = LOW voltage levels

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IH} Input voltage	-0.5 to +5.5	-0.5 to +7.0	V
I_{IH} Input current	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			UNIT
	Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage	2.0			2.0			V
V_{IL} LOW-level input voltage			+0.8			+0.8	V
I_{IK} Input clamp current			-12			-18	mA
I_{OH} HIGH-level output current			-800			-400	μ A
I_{OL} LOW-level output current			16			8	mA
T_A Operating free-air temperature	0		70	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	7442			74LS42			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$, $I_{OH} = \text{MAX}$	2.4	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$	0.2	0.4		0.35	0.5	V
		$I_{OL} = 4\text{mA}$ (74LS)				0.25	0.4	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$			-1.5			-1.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$		1.0				mA
		$V_I = 7.0\text{V}$					0.1	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$		40				μA
		$V_I = 2.7\text{V}$					20	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$			-1.6			-0.4	mA
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$	-18		-55	-20		-100	mA
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$		28	56		7	13	mA

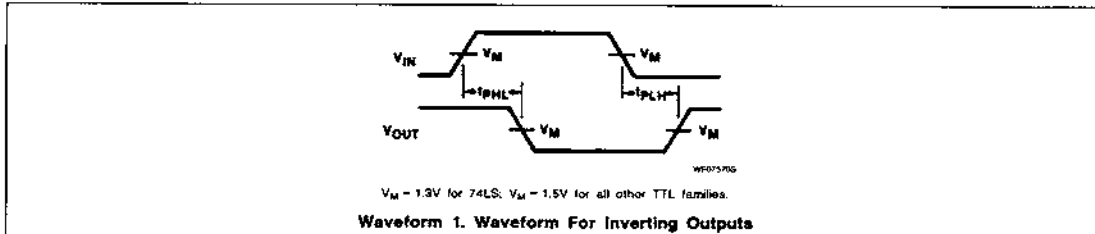
NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

3. I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC\text{ MAX}} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

4. I_{CC} is measured with all outputs open and all inputs grounded.

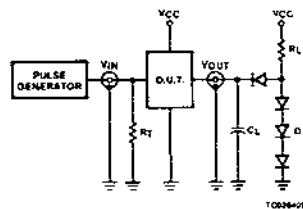
AC WAVEFORM**AC ELECTRICAL CHARACTERISTICS** $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			$C_L = 15\text{pF}, R_L = 409\Omega$		$C_L = 15\text{pF}, R_L = 2k\Omega$		
			Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1 3 logic levels		30		30	ns
t_{PHL}	Address to output			30		30	
t_{PLH}	Propagation delay	Waveform 1 2 logic levels		25		25	ns
t_{PHL}	Address to output			25		25	

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TEST CIRCUITS AND WAVEFORMS



Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

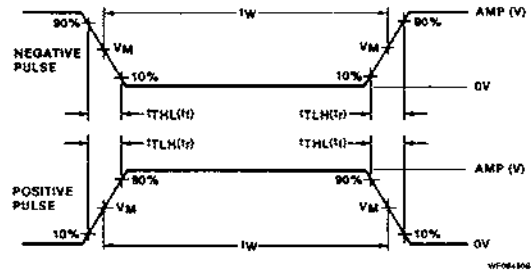
R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.



$V_M = 1.3V$ for 74LS, $V_M = 1.5V$ for all other TTL families.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns