Technical Overview

CD4000B Series

This section is intended as a guide for circuit and equipment designers in the operation and application of MOS integrated circuits. It covers general operating and handling considerations with respect to the following critical factors:

- Operating Supply Voltage Range
- Power Dissipation and Derating
- System Noise Considerations
- Power Source Rules
- Gate-oxide Protection Networks
- Input Signals and Ratings
- Chip Assembly and Storage
- Device Mounting
- Testing

More specific information is then given on significant features, special design and application requirements, and standard ratings and electrical characteristics for CMOS B-series logic circuits, and on CMOS special function circuits (special interface and display driver circuits).

General Operating and Handling Considerations

The following paragraphs discuss some key operating and handling considerations that must be taken into account to achieve maximum advantage of the CMOS technology. Additional information on the operation and handling of CMOS integrated circuits is given in Application Note AN6525, “Guide to Better Handling and Operation of CMOS Integrated Circuits”. See Section 8, “How to Use AnswerFAX”, in this selection guide.

Operating Supply Voltage Range

Because logic systems occasionally experience transient conditions on the power supply line which, when added to the nominal power-bus voltage, could exceed the safe limits of circuits connected to the power bus, the recommended operating supply voltage range is 3V to 18V for B-series devices. The recommended maximum power supply limit is substantially below the minimum primary breakdown limit for the devices to allow for limited power supply transient and regulation limits. For circuits that operated in a linear mode over a portion of the voltage range, such as RC or crystal oscillators, a minimum supply voltage of 4V is recommended.

Power Dissipation and Derating

The power dissipation of a CMOS integrated circuit is the sum of a DC (quiescent) component and an AC (dynamic) components. The DC component is the sum of the net integrated circuit reverse diode junction current and the surface leakage current times the supply voltage. In standard B-series logic devices, the DC dissipation typically ranges, depending upon device complexity, from 100nW to 400nW for a supply voltage of 10V. Worst-case DC dissipation is the product of the maximum quiescent current (given in the data sheet on each device) and the DC supply voltage V_{DD}.

Dynamic power dissipation has three components:

1. The dissipation that results from current that charges and discharges the external load capacitance of the output buffers. The dissipation of each output buffer is equal to CV^2f, where C is the load capacitance, V is the supply voltage, and f is the switching frequency of that output.
2. The dissipation that results from current that charges and discharges the internal node capacitances.
3. The dissipation caused by the current spikes through the PMOS and NMOS transistors in series at the instant of switching. This component amounts to approximately 10% of the total dissipation, shown graphically in the datasheets of most CMOS circuits.

All CMOS devices are rated at 200mW per package at the maximum operating ambient temperature rating (T_A) of 125°C for all packages. Power ratings for temperatures below the maximum operating temperature are shown in the standard CMOS thermal derating chart in Figure 1. This chart assumes that the device is mounted and soldered (or placed in a socket) on a PC board; there is natural convection cooling, with the PC board mounted horizontally; and the pressure is standard (14.7psia). In addition to the overall package dissipation, device dissipation per output transistor is limited to 100mW maximum over the full package operating temperature range.

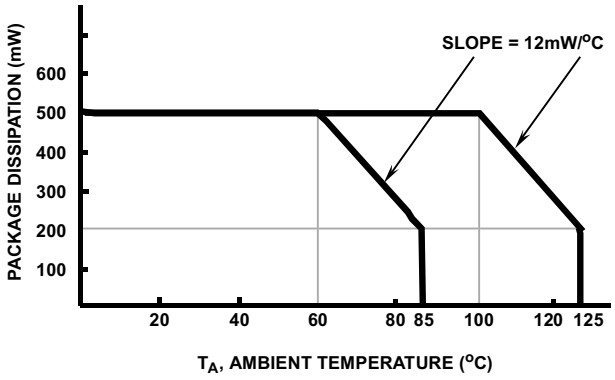


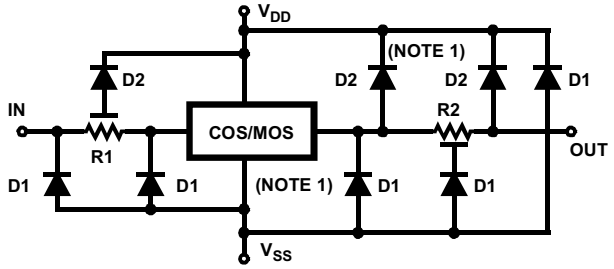
FIGURE 1. STANDARD CMOS THERMAL DERATING CHART

System Noise Considerations

In general, CMOS devices are much less sensitive to noise on power and ground lines than bipolar logic families (such as TTL or DTL). However, this sensitivity varies as a function of the power supply voltage, and more importantly as a function of synchronism between noise spikes and input transitions. Good power distribution in digital systems requires that the power bus have a low dynamic impedance; for this purpose, discrete decoupling capacitors should be distributed across the power bus. A more detailed discussion of CMOS noise immunity is provided by Application Note AN6587, “Noise Immunity of B-series CMOS Integrated Circuits”. See Section 8, “How to Use AnswerFAX”, in this selection guide.

Power Source Rules

Figure 2 shows the basic CMOS inverter and its gate-oxide protection network plus inherent diodes. The safe operating procedures listed below can be understood by reference to this inverter.



NOTES:

1. These Diodes are inherently part of the manufacturing process.
2. Diode Breakdown
   D1 ≈ 25V
   D2 ≈ 50V
   R2 << R1

FIGURE 2. BASIC CMOS INVERTER WITH B-SERIES TYPE PROTECTION NETWORK

1. When separate power supplies are used for the CMOS device and for the device inputs, the device power supply should always be turned on before the independent input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over dissipation and possible damage to the D2 input protection diode when the device power supply is grounded. When the device power supply is an open circuit, violation of this rule can result in undesired circuit operation although device damage should not result: AC inputs can be rectified by diode D2 to act as a power supply.
2. The power supply operating voltage should be kept safely below the absolute maximum supply rating, as indicated previously.
3. The power supply polarity for CMOS circuits should not be reversed. The positive (V_{DD}) terminal should never be more than 0.5V negative with respect to the negative (V_{SS}) terminal (V_{DD} - V_{SS} > -0.5V). Reversal of polarities will forward-bias and short the structural and protection diode between V_{DD} and V_{SS}.
4. V_{DD} should be equal to or greater than V_{CC} for CMOS buffers which have two power supplies (except for the CD40109B, and in particular, for CD4009 and CD4010 CMOS-to-TTL “down” conversion devices).
5. Power source current capability should be limited to as low a value as reasonable to assure good logic operation.
6. Large values of resistors in series with V_{DD} or V_{SS} should be avoided; transient turn-on of input protection diodes can result from drops across such resistors during switching.

Gate-Oxide Protection Network

A problem occasionally encountered in handling and testing low power semiconductor devices, including MOS and small geometry bipolar devices, has been damage to gate oxide and/or P-N junctions. Figure 3 shows the gate-oxide protection circuits used to protect CMOS devices from static electricity damage. Application Note AN6525, “Guide to Better Handling and Operation of CMOS Integrated Circuits”. See Section 8, “How to Use AnswerFAX”, in this selection guide.

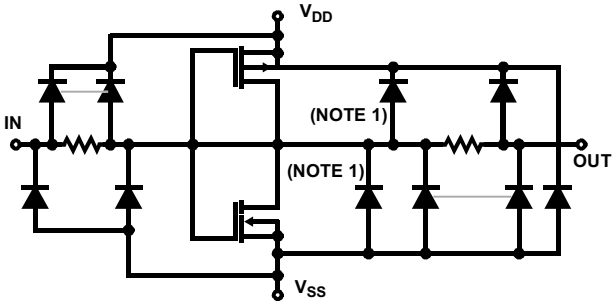


FIGURE 3A. FOR B-SERIES CMOS PRODUCT

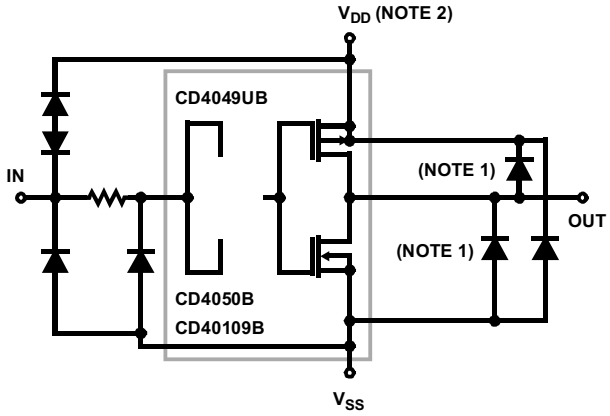


FIGURE 3B. FOR CD4049UB AND CD4050B AND CD40109B CMOS TYPES

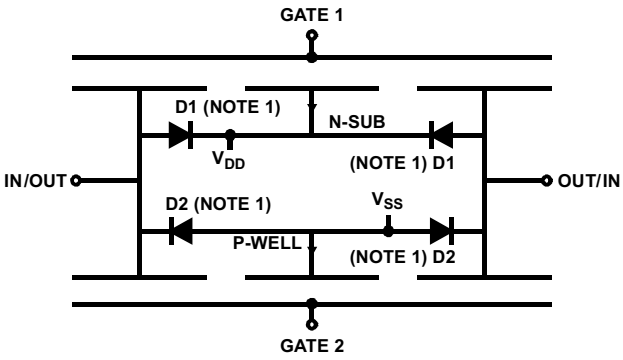


FIGURE 3C. FOR CMOS TRANSMISSION GATES

NOTES:

1. These Diodes are inherently part of the manufacturing process.
2. V_{CC} for CD4049UB and CD4050B
3. Diode Breakdown
   D1 ≈ 25V
   D2 ≈ 50V

FIGURE 3. GATE-OXIDE PROTECTION NETWORKS USED IN HARRIS CMOS INTEGRATED CIRCUITS

Input Signals and Ratings

Input signals should be maintained with in the power supply voltage range, $V_{SS} \le V_I \le V_{DD}$. If the input signal exceeds the recommended input signal swing range, the input current should be limited to ±100µA to minimize cross talk between input signals on adjacent terminals, and also to minimize any reduction in noise immunity.

The absolute maximum input current rating of ±10mA, shown in the published data, protects the device against the possible occurrence of an induced V_{DD} - V_{SS} latch condition, or damage to the input protection diodes. Latch-up conditions are explained in Application Note AN6525, “Guide to Better Handling and Operation of CMOS Integrated Circuits”. See Section 8, “How to Use AnswerFAX”, in this selection guide.

ALL CMOS inputs should be terminated. An exception can be made in the case of unbuffered NOR and NAND gates where terminating one of the series inputs to the proper polarity will not permit current flow caused by a floating input. Thus tying low one of the inputs of an unbuffered NAND gate, or tying high one of the inputs of an unbuffered NOR gate will satisfy this requirement.

When CMOS inputs are wired to edge card connectors with CMOS drive coming from another PC board, a shunt resistor in the range of 100kW should be connected to V_{DD} or V_{SS}, as applicable, in case the inputs become unterminated with the power supply on.

When CMOS circuits are driven by TTL logic, a “pull-up” resistor should be connected from the CMOS input to 5V (further information is given in Application Note AN6602, “Interfacing COS/MOS with Other Logic Families”, See Section 8, “How to Use AnswerFAX”, in this selection guide.

Output Rules

1. The power dissipation in a CMOS package should not exceed the rated value for the ambient temperature specified. The actual dissipation should be calculated when shorting outputs directly to V_{DD} or V_{SS}, driving low impedance loads, or directly driving the base of P-N-P or N-P-N bipolar transistor.
2. Output short circuits often result from testing errors or improper board assembly. Shorts on buffer outputs or across power supplies greater than 5V can damage CMOS devices.
3. CMOS, like active pull-up TTL, can be connected in the “wire-OR” configuration because an “on” PMOS and an “on” NMOS transistor could be directly shorted across the power supply rails. (Exception: CD40107B)
4. Paralleling inputs and outputs of gates is recommended only when the gates are within the same IC package.
5. Output loads should return to a voltage within the supply voltage range V_{DD} to V_{SS}.
6. Large capacitive loads (greater than 5000pF) on CMOS buffers or high current drivers act like short circuits and may over dissipate output transistors.
7. Output transistors may be over dissipated by operating buffers as linear amplifiers or using these types as one shot or astable multivibrators.

Noise immunity and Noise Margin

The complementary structure of the inverter, common to all CMOS logic devices, results in a near-ideal input-output transfer characteristic, with switching point midway (45% to 55%) between the 0 and 1 output logic levels. The result is high DC noise immunity.

Figure 4 shows a typical transfer curve that may be used to define the DC noise immunity of CMOS integrated circuits. The noise immunity voltage (V_{IL} or V_{IH}) is the noise voltage at any one input that does not propagate through the system. Minimum noise immunity for buffered B-series CMOS devices is 30%, 30%, and 27%, respectively for supply voltages V_{DD} of 5V, 10V, 15V and 20% of V_{DD} for all unbuffered gates. The V_{IL} and V_{IH} specifications define the maximum permissible additive noise voltage at an input terminal when input signals are within 50mV of the supply rails.

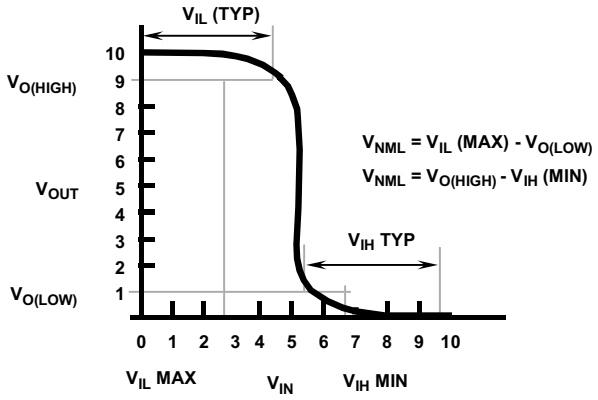


FIGURE 4. TYPICAL TRANSFER CURVE FOR A INVERTING GATE AT V_{DD} = 10V

Noise margin is the difference between the noise-immunity voltage (V_{IL} or V_{IH}) and the output voltage V_O. Noise margin voltage is the maximum voltage that can be impressed upon an input voltage V_{IN} (where V_{IN} is the V_{OL} or V_{OH} voltage of the preceding stage) at any (or all) logic I/O terminals without upsetting the logic or causing any output to exceed the output voltage (V_O) conditions specified for V_{IL} and V_{IH} ratings. Figure 5 illustrates the noise margin concept in a simple system. Minimum noise margins for buffered B-series CMOS devices are 1V, 2V, and 2.5V, respectively, for supply voltages 5V, 10V, and 15V.

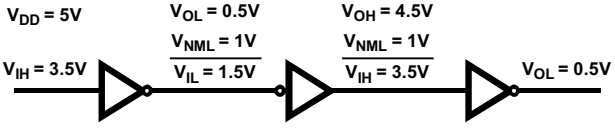


FIGURE 5. NOISE MARGIN EXAMPLE USING INVERTERS

Of the two noise limitation specifications (noise immunity and noise margin), noise immunity is more practical for CMOS devices because CMOS outputs are normally within 50mV of supply rails.

Noise immunity increases as the input pulse width becomes less than the propagation delay of the circuit. This condition is often described as AC noise immunity. Further information on noise immunity is given in Application Note AN6587, "Noise Immunity of B-series CMOS Integrated Circuits". See Section 8, "How to Use AnswerFAX", in this selection guide.

Clock Rise and Fall Time Requirements

Most CMOS clocked devices have maximum rise and fall time ratings (normally 5ms to 15ms). With longer rise or fall times, a device may not function properly because of data ripple through, false triggering problems, etc. Some B-series CMOS counters have Schmitt-trigger shaping circuits built into the clock circuit, removing the restriction for input rise or fall times. Long rise and fall times on CMOS buffer-type inputs cause increased power dissipation which may exceed device capability for operating power supply voltages greater than 5V.

Parallel Clocking

Process variations leading to differences in input threshold voltage among random device samples can cause loss of data between certain synchronously clock sequential circuits, as shown in Figure 6. This problem can be avoided if the maximum clock rise time ($t_R C_L$) for cascading any two CMOS sequential devices is limited in accordance with the following equation:

B-Series Types

$$\text{Maximum } t_R C_L = \frac{0.8 V_{DD}\,(V)}{1.15V} \times t_P\,(ns)$$

where $t_P = t_{PHL}$ or t_{PLH} (whichever is smaller) for the unit A in Figure 6 as specified on the device data sheet at the specified value of V_{DD} and loading conditions. Schmitt-trigger circuits such as the CD4093B are an ideal solution to applications requiring wave-shipping.

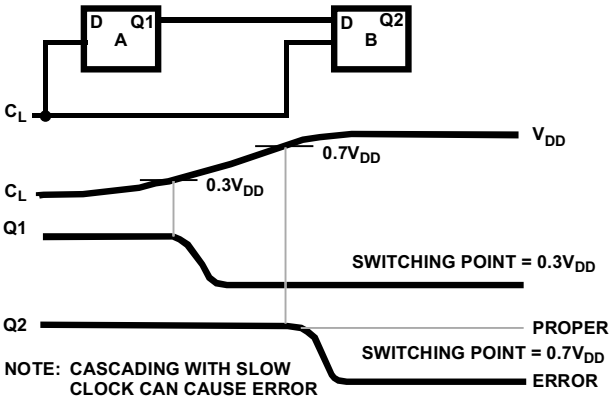


FIGURE 6. ERROR EFFECT THAT RESULTS FROM A SLOW CLOCK IN CASCADED CIRCUITS

Three-State Logic

Three-state logic can be easily implemented by use of a transmission gate in the output circuit; this technique provides a solution to the wire-OR problem in many cases.

Chip Assembly and Storage

Harris CMOS integrated circuits are provided in a chip from (H suffix) to allow customer design of special and complex circuits to suit individual needs. CMOS chips are electrically identical to and offer the features of their counterparts sealed in ceramic and plastic packages. The following paragraphs describe mounting considerations, packaging, shipping and storage criteria, handling criteria, visual inspection criteria, testing criteria, and bonding pad layout and dimensions for each chip.

Mounting Considerations

All CMOS chips are non-gold backed and require the use of epoxy mounting, conductive silver paste or equivalent is recommended. In any case the manufacturer's recommendations for storage and use should be followed.

In CMOS circuits MOS-transistor P-channel substrates (N-type bulk material) are connected to V_{DD}, therefore, when chips are mounted and a conductive paste is used, care must be taken to keep the active substrate isolated from ground or other circuit elements.

Packing, Shipping, and Storage Criteria

Solid-state chips, being small in size and unencapsulated, are physically fragile and require special handling consideration as follows:

- Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
  - Storage Temperature, 40°C Max
  - Relative Humidity, 50% Max
  - Clean, Dust-Free Environment
- The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
- During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
- After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to a moist and contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably affect their performance and/or reliability.

Handling Criteria

The user should find the following suggested precautions helpful in handling CMOS chips.

Because of the extremely small size and fragile nature of chips, the equipment designer should exercise care in handling these devices.

For additional handling considerations for CMOS devices, refer to Application Note AN6525, “Guide to Better Handling and Operation of CMOS Integrated Circuits”. See Section 8, “How to Use AnswerFAX”, in this selection guide.

- Grounding
  - Bonders, pellet pick-up tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip handling should be properly grounded.
  - The operator should be properly grounded.
- In-Process Handling
  - Assemblies or subassemblies of chips should be transported and stored in conductive carriers.
  - All external leads of the assemblies or subassemblies should be shorted together.
- Bonding Sequence
  - Connect V_{DD} first to external connections, for example, terminal 14 of the CD4001BH.
  - Remaining functions may be connected to their external connections in any sequence.
- Testing
  - Transport all assemblies of chips in conductive carriers.
  - In testing chip assemblies or subassemblies, the operator should be properly grounded.

Visual Inspection Criteria

All standard commercial CMOS chips undergo a visual inspection which is patterned after MIL-STD-883, Method 2010, Condition B with modifications reflecting CMOS requirements.

Testing Criteria

CMOS chips are DC electrically tested 100% in accordance with the same standards prescribed for Harris devices in standard packages.

Device Testing

Harris CMOS circuits are 100% tested by circuit probe in the wafer stage and are 100% tested again after they have been packaged. DC tests of Harris devices are performed at 5V, 10V, 15V, and 20V; functionality is checked at 2.8V, 17V, and 20V. Sample testing is used to assure adherence to quality requirements and AC specifications.

Static test, high speed functional and DC parametric tests, are performed at wafer and package stages by means of a Teradyne 325 test set or equivalent.

Users should follow the sequences below when testing CMOS devices:

1. Insert the device into the test socket.
2. Apply V_{DD}.
3. Apply the input signal.
4. Perform the test.
5. On completion of test, remove the input signal.
6. Turn off the power supply (V_{DD}).
7. Remove the device from the test socket and insert it into a conductive carrier. CMOS devices under test must not be exposed to electrostatic discharge or forward biasing of the intrinsic protective diodes shown in Figure 3.

Detailed information on the techniques employed in the testing of Harris CMOS integrated circuits are described in Application Note AN6532, “Fundamentals of Testing CMOS Integrated Circuits”. See Section 8, “How to Use AnswerFAX”, in this selection guide.

Device Mounting

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with nickel-plated Kovar leads (See MIL-I-38535). It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead. It is also extremely important that the ends of bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

High Voltage B-Series CMOS Integrated Circuits

Harris CD4000B series types have a maximum DC supply voltage rating of -0.5V to 20V, and a recommended operating supply voltage range of 3V to 18V. The major features of this series are as follows:

- High Voltage (20V) Ratings
- 100% Tested for Quiescent Current at 20V
- 5V, 10V, and 15V Parametric Ratings
- Standardized, Symmetrical Output Characteristics
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and 25°C
- Noise Margin (Full Package Temperature Range) =
  1V at V_{DD} = 5V
  2V at V_{DD} = 10V
  2.5 V at V_{DD} = 15V
- Meets all requirements of JEDEC Tentative Standard No. 13B, “Standard Specifications for Description of B-Series CMOS Devices”.

JEDEC Minimum Standard

Under the sponsorship of the Joint Electron Devices Engineering Council (JEDEC) of the Electronic Industries Association (EIA), minimum industrial standards have been established for the maximum ratings, DC and AC electrical

characteristics of B-series CMOS integrated circuits. The JEDEC standard (JEDEC Tentative Standard No. 13B) defines B-series CMOS integrated circuits as a uniform family of both buffered and unbuffered types that have an absolute DC supply voltage rating of at least 18V.

Buffered CMOS Devices

These are types in which the output "on" impedance is independent of any and all valid input logic conditions, both preceding and present. All such CMOS products are designated by suffix "B" following the basic type number.

Unbuffered CMOS Devices

These are types that meet all B-series specifications except that the logical outputs are not buffered and the noise-immunity voltages, V_{IL} and V_{IH}, are specified as 20% and 80%, respectively, of V_{DD} for operation from 5V, 10V, and 17V and 83%, respectively, of V_{DD} for operation from 15V. All such CMOS product are designated by the suffix "UB".

The JEDEC minimum standard also includes in the B-series, CMOS types that have analog inputs or outputs and in addition, have maximum ratings and logical input and output parameters that conform to B-series specifications wherever applicable. These CMOS devices are also designated by the suffix "B".

All B-series CMOS devices can directly replace their A-series counterparts in most applications. The UB types are high voltage versions of corresponding A-series (unbuffered) types.

Commercial A-series types have been obsoleted and replaced by B-series counterparts with only a few exceptions such as the continuing CD4059A types.

The **Absolute Maximum Rating - JEDEC** table lists the minimum standards established for the maximum ratings and recommended operating conditions for B-series CMOS integrated circuits.

The **DC Electrical Specification - JEDEC** table shows the JEDEC standards for the DC electrical specifications of CMOS B-series integrated circuits.

Standardized Ratings and Static Characteristics

Harris B-series CMOS integrated circuits meet or exceed the most stringent requirements of the JEDEC B-series specifications. The **Absolute Maximum Ratings** table shows the standardized maximum ratings and recommended operating supply voltage range for Harris B-series CMOS integrated circuits. The standardized DC electrical specifications for these devices are shown in the **DC Electrical Specification** table. As with the JEDEC specifications, the Harris standardized characteristics classify the B-series devices into three leakage (quiescent device current) categories. Table 1 lists the Harris types in each category and indicates types that, although they are still B-series types, differ in one or more static characteristics.

The **Absolute Maximum Ratings** table and the **DC Electrical Specification** table show that in a number on important respects, Harris has established new performance standards for B-series CMOS logic circuits.

- Tight Limits For All Packages

  Harris devices used the same set of limits for all package styles. The JEDEC standard establishes two sets of limits for most DC parameters; a tight set for products having a full operating temperature range of -55°C to +125°C (all Harris devices), and a relaxed set for products having a limited temperature range of -40°C to +85°C. Because Harris supplies only one premium grade of B-series product in all package styles (i.e., fall-out chips are not used), all B-series CMOS devices are specified to the tight set of limits only.

- Improved Voltage Rating

  All Harris B-series devices are tested to voltages that insure safe operation at the absolute maximum DC supply voltage rating of 20V. This higher rating permits greater derating for reliable 15V operation, permits greater 15V supply tolerance and peak transients, and permits system use to 18V with confidence.

- Wider Operating Range

  All Harris B-series devices have a recommended maximum operating voltage of 18V. The higher limit permits 18V system supply operation, and also permits wider power source tolerance and transients for supplies normally set up to 18V

- Lower Leakage Current

  The JEDEC standard establishes three sets of limits for quiescent device current (I_{DD}) intended to match chip complexity to device leakage current as realistically as possible.

  For all three levels of chip complexity, all Harris B-series devices (regardless of package) conform to the tighter set of limits established in the standard. In addition, a maximum rating is specified at 20V, as well as at 5V, 10V, and 15V. As a result:

  - In current limited applications, CMOS users can depend on one tight leakage limit independent of package style selected.
  - Customer use of CMOS product up through 18V is protected by a published tight leakage current specification at 20V (as well as by an input leakage specification at 18V).

- Symmetrical Output

  Most Harris B-series devices have balanced complementary output drive (i.e., the output high current I_{OH} rating is the same as the output low current I_{OL} rating specified to the tighter set of limits established in the JEDEC standard. The balanced output provides uniform rise and fall time performance, improved system noise energy (dynamic) immunity, optimum device speed for both output switching low-to-high (t_{PLH}) and output switching high-to-low (t_{PHL}), and in general the identical high and low DC and AC characteristics normally associated with a good complementary output drive circuit. MOS system design, simulation, and performance are significantly enhanced by equal high and low DC and AC performance ratings and one tight specification limit for all package styles.

- Improved Input Current (Leakage) Ratings

  All Harris B-series devices (regardless of package) have a maximum input leakage current (I_{IN}) rating of 100nA specified at voltages up to 18V, and a maximum limit of 1µA at the upper limit of the package temperature range. Actually, the 100nA rating is a practical specification limited by the inability of commercial test equipment to measure lower currents. Laboratory tests show that input leakage currents of Harris B-series CMOS devices are significantly lower than this limit, typically ranging from 10pA to 100pA.

- Buffered and Unbuffered Gates

  The new industry standard establishes a suffix “UB” for CMOS products that meet all B-series specifications except that the logical outputs of the devices are not buffered and the V_{IL} and V_{IH} specifications are relaxed. The suffix “B” defines only buffered output devices in which the output “on” impedance is independent of any and all valid input logic conditions, both preceding and present.

  Harris supplies both buffered “B” and unbuffered “UB” versions of a few popular NOR and NAND gates to make available to designers the advantages of both. The following table briefly compares the features of the two versions, a more detailed coverage of the special features of B- and UB- series CMOS gates is provided by Application Note AN6558, “Understanding Buffered and Unbuffered CMOS Characteristics”. See Section 8, “How to Use AnswerFAX”, in this selection guide.

COMPARISON OF “B” AND “UB”

CHARACTERISTIC	BUFFERED VERSION “B”	UNBUFFERED VERSION “UB”
Propagation Delay (Speed)	Moderate	Fast
Noise Immunity/Margin	Excellent	Good
Output Impedance and Output Transition Time	Constant	Variable
AC Gain	High	Medium
Output Oscillation for Slow inputs	Yes	No
Input Capacitance	Low	High

- Reliability

  Harris B-series CMOS integrated circuits incorporate the latest improvements in processing technology and plastic and ceramic packaging techniques. Product quality is real time controlled using accelerated temperature group quality screening in which measured DC parameters are criticized against tight B-series limits.

  Figure 7 through Figure 10 show the standardized N- and P-channel drain characteristics for B-series CMOS devices, and Figure 11 through Figure 14 show the normalized variation of output source and sink currents with respect to temperature and voltage in these devices.

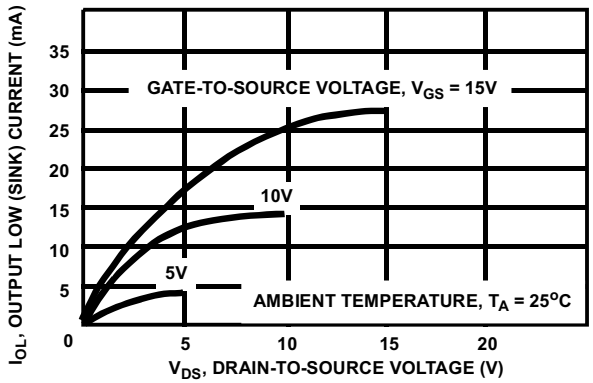


FIGURE 7. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

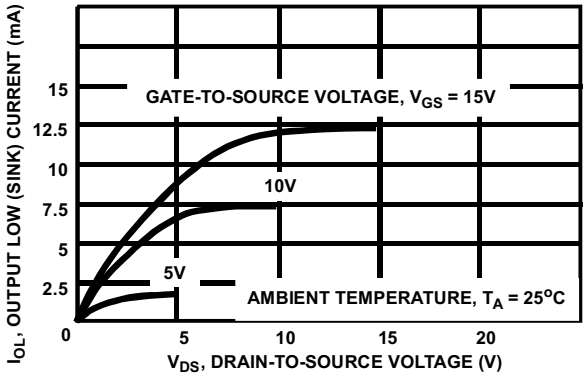


FIGURE 8. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

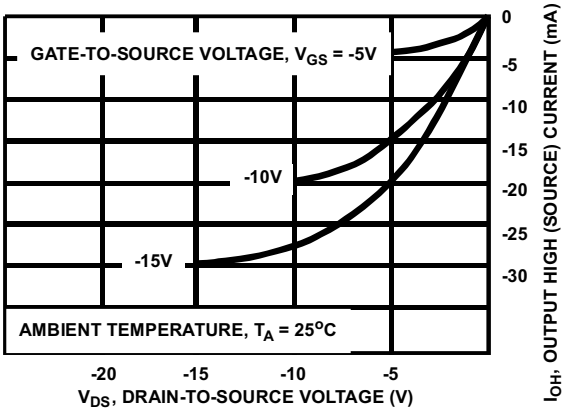


FIGURE 9. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

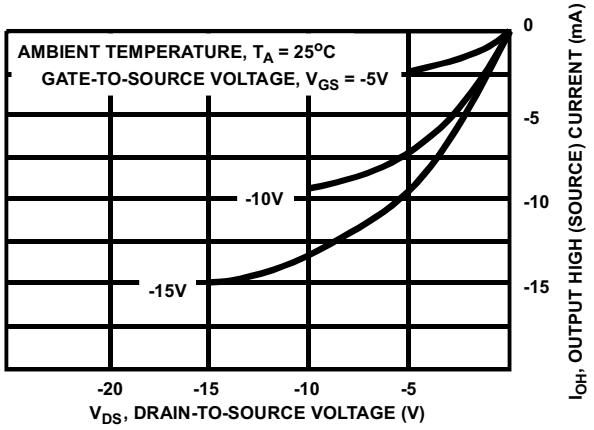


FIGURE 10. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

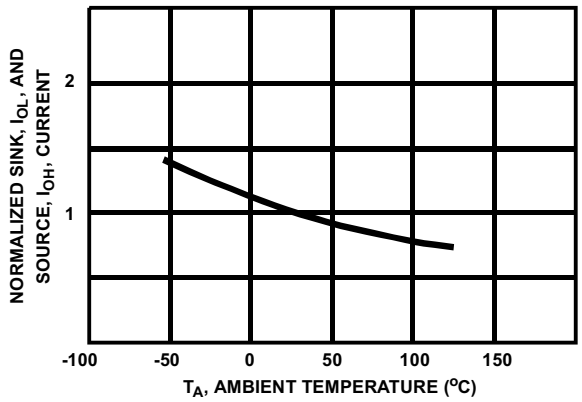


FIGURE 11. VARIATION OF NORMALIZED OUTPUT LOW (SINK) CURRENT I_{OL} AND OUTPUT HIGH (SOURCE) CURRENT I_{OH} WITH TEMPERATURE

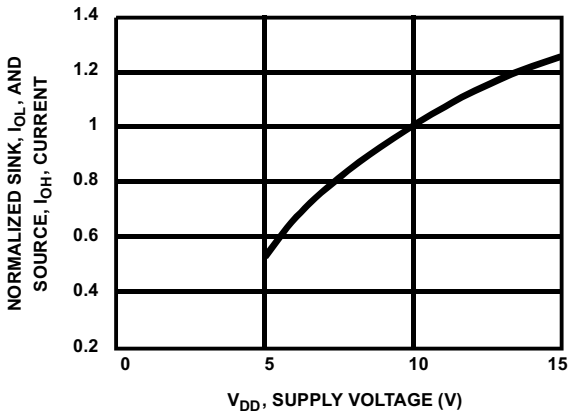


FIGURE 12. VARIATION OF NORMALIZED OUTPUT LOW (SINK) CURRENT I_{OL} AND OUTPUT HIGH (SOURCE) CURRENT I_{OH} WITH SUPPLY VOLTAGE

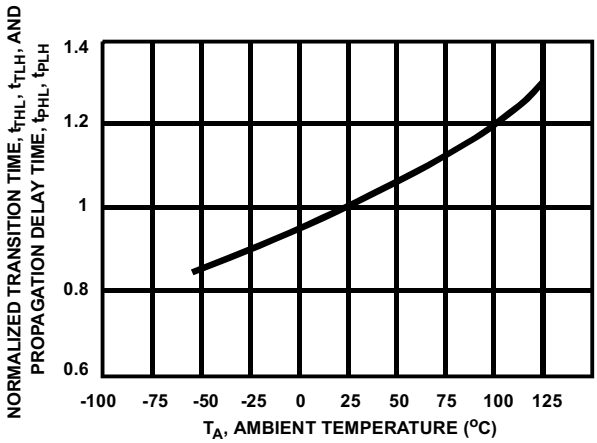


FIGURE 13. VARIATION OF LOW-TO-HIGH (t_{TLH}) AND HIGH-TO-LOW (t_{THL}) TRANSITION TIME, AND LOW-TO-HIGH (t_{PHL}) PROPAGATION DELAY TIME WITH TEMPERATURE

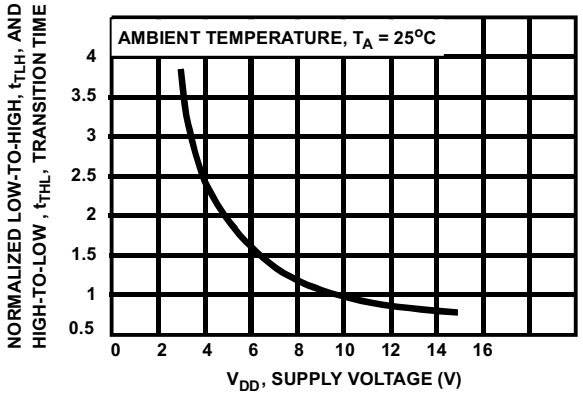


FIGURE 14. VARIATION OF LOW-TO-HIGH (t_{TLH}) AND HIGH-TO-LOW (t_{THL}) TRANSITION TIME WITH SUPPLY VOLTAGE

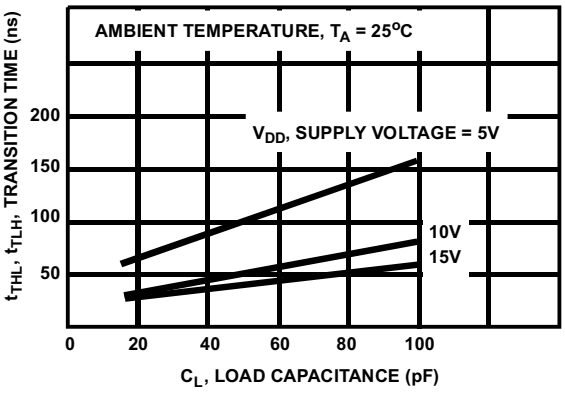


FIGURE 15. VARIATION OF TRANSITION TIME (t_{THL}, t_{TLH}) WITH LOAD CAPACITANCE

B-Series AC Electrical Specifications

B-series AC electrical specifications for individual types are under the following conditions: V_{DD} = 5V, 10V, and 15V; T_A = +25°C; C_L = 50pF; R_L = 200kΩ; t_R and t_F = 20ns. Figure 13 shows the variation of B-series AC parameter with temperature. Figure 14 shows the variation of output transition time with supply voltage. Figure 17 shows the variation of the standardized output transition time with load capacitance.

Maximum propagation delay or transition times for values of C_L other than the specified 50pF can be determined by use of the multiplication factor (usually 2) between the typical and maximum values given in the AC specifications chart included in the technical data for each device applied to the typical curves, and also shown in the device technical data.

B-Series AC Switching Specifications

The **AC Electrical Specification** table defines the major CMOS AC specifications, with reference to the waveforms shown in Figure 16 through Figure 19. Test conditions of V_{DD}, low capacitance (C_L), and input conditions are given for individual types in the published data.

CMOS Special Products

Harris supplies some special CMOS products that have operating supply voltage ranges and other characteristics that differ from the standardized data specified for B-series CMOS integrated circuits.

These special application types include: interface circuits for level shifting applications to interface CMOS logic levels with different logic types; display drivers non-multiplexed, 4 digit, 7 segment LCD types containing all the circuitry necessary for driving conventional LCD displays without the need for external components, and a video sync generator function.

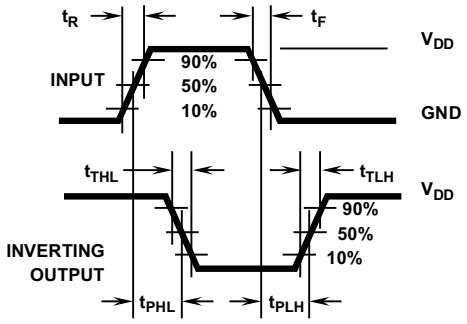
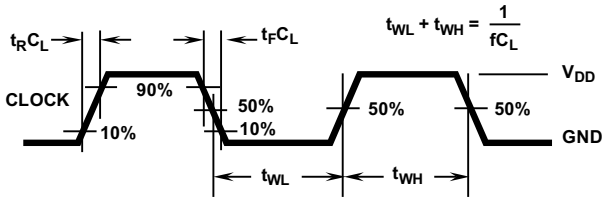


FIGURE 16. TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC



NOTE: Outputs should be switching from 10% V_{DD} to 90% V_{DD} in accordance with the device truth table.

FIGURE 17. CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

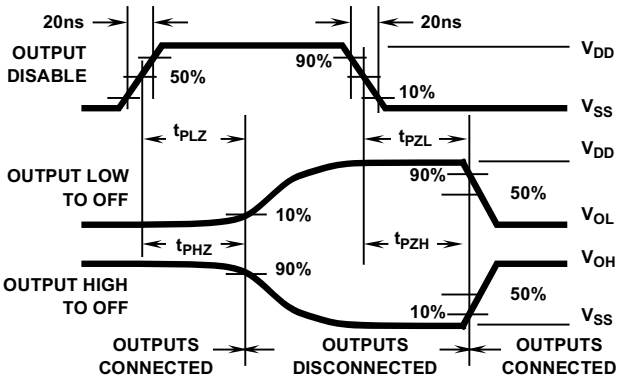


FIGURE 18A.

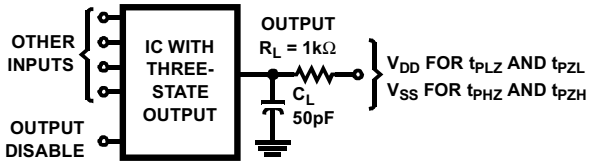
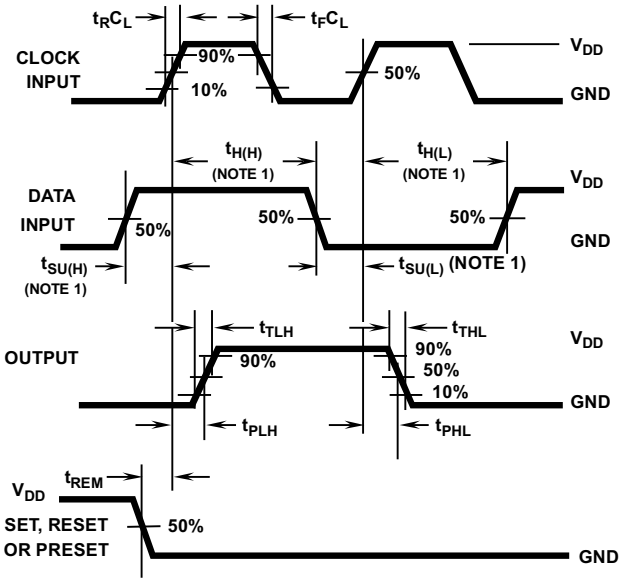


FIGURE 18B.

FIGURE 18. THREE-STATE PROPAGATION DELAY WAVE SHAPES AND TEST CIRCUIT



NOTE:

1. (H) or (L) Optional

FIGURE 19. SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

Family Ratings and Specifications‡

Absolute Maximum Ratings

JEDEC Standard for DC Specifications of B-Series CMOS Integrated Circuits (Note 1 and Note 2)

DC Supply Voltage, V_{DD} . . . . . -0.5V to +18V
DC Input Voltage, V_{IN} . . . . . -0.5V to V_{DD} +0.5V
DC Input Current, I_{IN} (For Any One Input). . . . . ±10mA
Storage Temperature, T_S . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

DC Supply Voltage, V_{DD} . . . . . +3V to +15V
Operating Temperature Range, T_A . . . . . -55°C to +125°C

DC Electrical Specification

JEDEC Standard for DC Specifications of B-Series CMOS Integrated Circuits

PARAMETERS	SYMBOL	TEST CONDITIONS	TEMP. RANGE	V_{DD} (V)	(NOTE 3) T_{LOW}		+25°C			(NOTE 4) T_{HIGH}		UNIT
					MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Quiescent Device Current	I_{DD}	$V_{IN} = V_{SS}$ or V_{DD} All Valid Input Combinations	Mil	5	-	0.25	-	-	0.25	-	7.5	µA
				10	-	0.5	-	-	0.5	-	15	µA
Gates				15	-	1	-	-	1	-	30	µA
			Comm	5	-	1	-	-	1	-	7.5	µA
				10	-	2	-	-	2	-	15	µA
				15	-	4	-	-	4	-	30	µA
Buffers, Flip-Flops	I_{DD}	$V_{IN} = V_{SS}$ or V_{DD} All Valid Input Combinations	Mil	5	-	1	-	-	1	-	30	µA
				10	-	2	-	-	2	-	60	µA
				15	-	4	-	-	4	-	120	µA
			Comm	5	-	4	-	-	4	-	30	µA
				10	-	8	-	-	8	-	60	µA
				15	-	16	-	-	16	-	120	µA
MSI	I_{DD}	$V_{IN} = V_{SS}$ or V_{DD} All Valid Input Combinations	Mil	5	-	5	-	-	5	-	150	µA
				10	-	10	-	-	10	-	300	µA
				15	-	20	-	-	20	-	600	µA
			Comm	5	-	20	-	-	20	-	150	µA
				10	-	40	-	-	40	-	300	µA
				15	-	80	-	-	80	-	600	µA
Low Level Output Voltage	V_{OL}	$V_{IN} = V_{SS}$ or V_{DD} $\|I_O\| < 1µA$	All	5	-	0.05	-	-	0.05	-	0.05	V
				10	-	0.05	-	-	0.05	-	0.05	V
				15	-	0.05	-	-	0.05	-	0.05	V
High Level Output Voltage	V_{OH}	$V_{IN} = V_{SS}$ or V_{DD} $\|I_O\| < 1µA$	All	5	4.95	-	4.95	-	-	4.95	-	V
				10	9.95	-	9.95	-	-	9.95	-	V
				15	14.95	-	14.95	-	-	14.95	-	V

‡ For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

Family Ratings and Specifications‡

DC Electrical Specification JEDEC Standard for DC Specifications of B-Series CMOS Integrated Circuits **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	TEMP. RANGE	V_{DD} (V)	(NOTE 3) T_{LOW}		+25°C			(NOTE 4) T_{HIGH}		UNIT
					MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Input Low Voltage B Types	V_{IL}	V_O = 0.5V or 4.5V V_O = 1V or 9V V_O = 1.5V or 13.5V $\|I_O\|$ <1µA	All	5	-	1.5	-	-	1.5	-	1.5	V
				10	-	3	-	-	3	-	3	V
				15	-	4	-	-	4	-	4	V
UB Types				5	-	1	-	-	1	-	1	V
				10	-	2	-	-	2	-	2	V
				15	-	2.5	-	-	2.5	-	2.5	V
Input High Voltage B Types	V_{IH}	V_O = 0.5V or 4.5V V_O = 1V or 9V V_O = 1.5V or 13.5V $\|I_O\|$ <1µA	All	5	3.5	-	3.5	-	-	3.5	-	V
				10	7	-	7	-	-	7	-	V
				15	11	-	11	-	-	11	-	V
UB Types				5	4	-	4	-	-	4	-	V
				10	8	-	8	-	-	8	-	V
				15	12.5	-	12.5	-	-	12.5	-	V
Output Low (Sink) Current	I_{OL}	V_O = 0.4V V_{IN} = 0V or 5V V_O = 0.5V V_{IN} = 0V or 10V V_O = 1.5V V_{IN} = 0V or 15V	Mil	5	0.64	-	0.51	-	-	0.36	-	mA
				10	1.6	-	1.3	-	-	0.9	-	mA
				15	4.2	-	3.4	-	-	2.4	-	mA
			Comm	5	0.52	-	0.44	-	-	0.36	-	mA
				10	1.3	-	1.1	-	-	0.9	-	mA
				15	3.6	-	3.0	-	-	2.4	-	mA
Output High (Source) Current	I_{OH}	V_O = 4.6V V_{IN} = 0V or 5V V_O = 9.5V V_{IN} = 0V or 10V V_O = 13.5V V_{IN} = 0V or 15V	Mil	5	-0.25	-	-0.2	-	-	-0.14	-	mA
				10	-0.62	-	-0.5	-	-	-0.35	-	mA
				15	-1.8	-	-1.5	-	-	-1.1	-	mA
			Comm	5	-0.2	-	-0.16	-	-	-0.12	-	mA
				10	-0.5	-	-0.4	-	-	-0.3	-	mA
				15	-1.4	-	-1.2	-	-	-1.0	-	mA
Input Current	I_{IN}	V_{IN} = 0V or 15V	Mil	15	-	±0.1	-	-	±0.1	-	±1	µA
		V_{IN} = 0V or 15V	Comm	15	-	±0.3	-	-	±0.3	-	±1	µA
Three-State Output Leakage Current	I_{OUT} Max	V_{IN} = 0V or 15V	Mil	15	-	±0.4	-	-	±0.4	-	±12	µA
		V_{IN} = 0V or 15V	Comm	15	-	±1.6	-	-	±1.6	-	±12	µA
Input Capacitance Per Unit Load	C_{IN}	Any Input	All	-	-	-	-	-	7.5	-	-	pF

NOTES:

1. Voltages referenced to V_{SS}.
2. Reprinted from JEDEC Standard No. 13-B, “JEDEC Standard Specification for Description of B-Series CMOS Devices”.
3. T_{LOW} = -55°C for Military Temperature Range Device, -40°C for Commercial Temperature Device (All Harris Devices).
4. T_{HIGH} = +125°C for Military Temperature Range Device, +85°C for Commercial Temperature Range Device.

‡ For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, “How to use AnswerFAX”, in this selection guide.

Family Ratings and Specifications‡

Standardized Absolute Maximum Ratings For B-Series CMOS Integrated Circuits

DC Supply Voltage, V_{DD}
Voltage Reference to V_{SS} Terminal. . . . . -0.5V to +20V
Input Voltage, All Inputs . . . . . -0.5V to V_{DD} +0.5V
DC Input Current,
For Any One Input. . . . . ±10mA
Lead Temperature (During Soldering)
At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)
from Case for 10s Max . . . . . +265°C

Power Dissipation Per, P_D
T_A = -55°C to +100°C 500mW
T_A = +100°C to +125°C . . . Derate Linearly at 12mW/°C to 200mW
Device Dissipation Per Output Transistor
For T_A = Full Package Temperature Range
(All Package Test) 100mW
Operating Temperature Range, T_A . . . . . -55°C to +125°C
Storage Temperature, T_{STG} . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Supply, Voltage Range
For T_A = Full Package Temperature Range . . . . . +3V to +18V

Standardized DC Electrical Specification For B-Series CMOS Integrated Circuits

PARAMETERS	SYMBOL	TEST CONDITIONS			LIMITS				+25°C			UNIT
		V_O (V)	V_{IN} (V)	V_{DD} (V)	-55°C	-40°C	+85°C	+125°C	MIN	TYP	MAX	
Quiescent Device Current	I_{DD} Max	-	0, 5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	µA
		-	0, 10	10	0.5	0.5	15	15	-	0.01	0.5	µA
Gates, Inverters (Note 1)		-	0, 15	15	1	1	30	30	-	0.01	1	µA
		-	0, 20	20	5	5	150	150	-	0.02	5	µA
Buffers, Flip-Flops, Latches, Multi-Level Gates (MSI-1 Types) (Note 1)		-	0, 5	5	1	1	30	30	-	0.02	1	µA
		-	0, 10	10	2	2	60	60	-	0.02	2	µA
		-	0, 15	15	4	4	120	120	-	0.02	4	µA
		-	0, 20	20	20	20	600	600	-	0.04	20	µA
Complex Logic (MSI-2 Types) (Note 1)		-	0, 5	5	5	5	150	150	-	0.04	5	µA
		-	0, 10	10	10	10	300	300	-	0.04	10	µA
		-	0, 15	15	20	20	600	600	-	0.04	20	µA
		-	0, 20	20	100	100	3000	3000	-	0.08	100	µA
Output Low (Sink) Current Min	I_{OL} Min	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
		0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	mA
		1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	-	mA
Output High (Source) Current, Min	I_{OH} Min	4.6	0, 5	5	-6.4	-0.61	-0.42	-0.36	-0.51	-1	-	mA
		2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	mA
		9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	mA
		13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	mA

‡ For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, "How to use AnswerFAX", in this selection guide.

Standardized DC Electrical Specification For B-Series CMOS Integrated Circuits **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS			LIMITS				+25°C			UNIT
		V_O (V)	V_{IN} (V)	V_{DD} (V)	-55°C	-40°C	+85°C	+125°C	MIN	TYP	MAX	
Output Voltage Low-Level	V_{OL} Max	-	0, 5	5	0.05				-	0	0.05	V
		-	0, 10	10	0.05				-	0	0.05	V
		-	0, 15	15	0.05				-	0	0.05	V
Output Voltage High-Level	V_{OH} Min	-	0, 5	5	4.95				4.95	5	-	V
		-	0, 10	10	9.95				9.95	10	-	V
		-	0, 15	15	14.95				14.95	15	-	V
Input Low Voltage	V_{IL} Max	0.5, 4.5	-	5	1.5				-	-	1.5	V
		1, 9	-	10	3				-	-	3	V
B Types		1.5, 13.5	-	15	4				-	-	4	V
UB Types		0.5, 4.5	-	5	1				-	-	1	V
		1, 9	-	10	2				-	-	2	V
		1.5, 13.5	-	15	2.5				-	-	2.5	V
Input High Voltage	V_{IH} Max	0.5, 4.5	-	5	3.5				3.5	-	-	V
		1, 9	-	10	7				7	-	-	V
B Types		1.5, 13.5	-	15	11				11	-	-	V
UB Types		0.5, 4.5	-	5	4				4	-	-	V
		1, 9	-	10	8				8	-	-	V
		1.5, 13.5	-	15	12.5				12.5	-	-	V
Input Current	I_{IN} Max	-	0, 18	18	±0.1	±0.1	±1	±1	-	$±10^{-5}$	±0.1	µA
Three-State Output Leakage Current	I_{OUT} Max	0, 18	0, 18	18	±0.4	±0.4	±12	±12	-	$±10^{-4}$	±0.4	µA

NOTE:

1. Classifications of Harris CMOS B-Series Types are Shown in Table 1.

‡ For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, “How to use AnswerFAX”, in this selection guide.

AC Electrical Specifications Definitions

PARAMETERS	SYMBOL	MIN	MAX	NOTES
PROPAGATION DELAY				
Outputs Going High to Low	t_{PHL}	-	X	-
Outputs Going Low to High	t_{PLH}	-	X	-
OUTPUT TRANSITION TIME				
Outputs Going High to Low	t_{THL}	-	X	-
Outputs Going Low to High	t_{TLH}	-	X	-
PULSE WIDTH				
Set, Reset, Preset, Enable, Disable, Strobe, Clock	t_{WL} or t_{WH}	X	-	1
Clock Input Frequency	f_{CL}	-	X	1, 2
Clock Input Rise and Fall Time	t_{RCL}, t_{FCL}	-	X	-
Set-Up Time	t_{SU}	X	-	1
Hold Time	t_H	X	-	1
Removal Time - Set, Reset, Preset-Enable	t_{REM}	X	-	1
THREE-STATE DISABLE DELAY TIMES				
High Level to High Impedance	t_{PHZ}	-	X	-
High Impedance to Low Level	t_{PZL}	-	X	-
Low Level to High Impedance	t_{PLZ}	-	X	-
High Impedance to High Level	t_{PZH}	-	X	-

NOTES:

1. By placing a defining Min or Max in front of definition, the limits can change from Min to Max, or vice versa.
2. Clock input waveform should have a 50% duty cycle and be such as to cause the Outputs to be switching from 10% V_{DD} to 90% V_{DD} in accordance with the device truth table.

TABLE 1. CLASSIFICATION OF HARRIS B-SERIES CMOS INTEGRATED CIRCUITS ACCORDING TO CIRCUIT COMPLEXITY

GATES/INVERTERS		BUFFERS/FLIP-FLOP/ LATCHES/MULTI-LEVEL GATES (MSI-1)		COMPLEX LOGIC (MSI-2)		
CD4001B	CD4069UB	CD4009UB (Note 1)	C04093B	CD4006B	CD4055B (Note 1)	CD4532B
CD4001UB	CD4070B	CD4010B (Note 1)	CD4095B	CD4008B	CD4056B (Note 1)	CD4536B
CD4002B	CD4071B	CD4013B	CD4096B	CD4014B	CD4060B	CD4541B
CD4007UB	CD4072B	CD4019B	CD4098B	CD4015B	CD4063B	CD4543B
CD4011B	CD4073B	CD4027B	CD4502B (Note 1)	CD4017B	CD4067B (Note 1)	CD4555B
CD4011UB	CD4075B	CD4030B	CD4503B	CD4018B	CD4076B	CD4556B
CD4012B	CD4077B	CD4041UB (Note 1)	CD4504B	CD4020B	CD4089B	CD4560B

‡ For specific technical information on each individual device type, refer to the appropriate data sheet in Harris AnswerFAX. See Section 8, “How to use AnswerFAX”, in this selection guide.

TABLE 1. CLASSIFICATION OF HARRIS B-SERIES CMOS INTEGRATED CIRCUITS ACCORDING TO CIRCUIT COMPLEXITY (Continued)

GATES/INVERTERS		BUFFERS/FLIP-FLOP/ LATCHES/MULTI-LEVEL GATES (MSI-1)		COMPLEX LOGIC (MSI-2)		
CD4016B (Note 1)	CD4078B	CD4042B	CD4519B	CD4021B	CD4094B	CD4566B
CD4023B	CD4081B	CD4043B	CD40106B	CD4022B	CD4097B (Note 1)	CD4585B
CD4025B	CD4082B	CD4044B	CD40107B (Note 1)	CD4024B	CD4099B	CD4724B
CD4048B	CD40117B	CD4047B	CD40109B (Note 1)	CD4026B	CD4508B	CD14538B
CD4066B (Note 1)	CD4572UB	CD4049UB (Note 1)	CD40174B	CD4028B	CD4510B	CD40100B
CD4068B		CD4050B (Note 1)	CD40175B	CD4029B	CD4511B (Note 1)	CD40102B
		CD4085B	CD40257B	CD4031B	CD4512B	CD40103B
		CD4086B		CD4033B	CD4514B	CD40105B
				CD4034B	CD4515B	CD40110B (Note 1)
				CD4035B	CD4516B	CD40147B
				CD4040B	CD4517B	CD40160B
				CD4045B (Note 1)	CD4518B	CD40161B
				CD4046B (Note 1)	CD4520B	CD40163B
				CD4051B (Note 1)	CD4521B	CD40192B
				CD4052B (Note 1)	CD4522B	CD40193B
				CD4053B (Note 1)	CD4527B	CD40194B
				CD4054B (Note 1)	CD4529B	

NOTE:

1. Indicates types for which, because of special design requirements, one or more static characteristics differ from the standardized data. Refer to data pages on these types for specific differences.

Enhanced Product

STANDARD IC CIRCUITS

		SUFFIX "X"
Burn-In Time (Note 1)		160 Hours
Temperature (Note 1)		+125°C
Bias Voltage	CD4000B	15V
	Special	Differs by Type

PRODUCT IDENTIFICATION	
All Enhanced Product is Identified by a Suffix "X"	
Examples: Standard CD4001BE	Enhanced CD4001BEX

NOTE:

1. Or equivalent means equivalent time-temperature /voltage resulting in the same activation energy.

PRODUCT FLOW