ISO-CMOS MD65SC51B Asynchronous Communications Interface Adaptor

9161-002-052 NA ISSUE 5 November 1990

Features

- Replacement for existing NMOS part.
- 15 selectable baud rates from 50 bit/s to 19.2 kbit/s or 1/16th of an external clock rate.
- Selectable word length & number of stop bits.
- Selectable echo mode.
- Full or half duplex operation.
- Data set/modem control functions.
- Parity generation and checking.
- Low power ISO-CMOS technology.
- TTL compatible.
- Single 3-6 volt power supply.

Applications

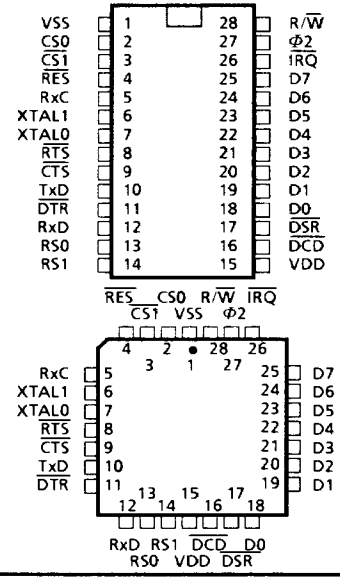
- Microprocessor to modem bidirectional link.
- Microprocessor (µP) serial data interface.
- Serial input/output interface.

Description

The MD65SC51B is an Asynchronous Communications Interface Adaptor fabricated in Mitel's ISO-CMOS technology. The device provides interfacing between a µP and a modem.

The MD65SC51B will also control all of the interrupt handling between the µP and the modem. An on-board baud rate generator is available to derive one of 15 selectable baud rates or 1/16th of an external clock rate.

Pin Connections



Ordering Information -40° to 85°C

MD65SC51BE	28 Pin PLASTIC DIP
MD65SC51BP	28 Pin PLCC

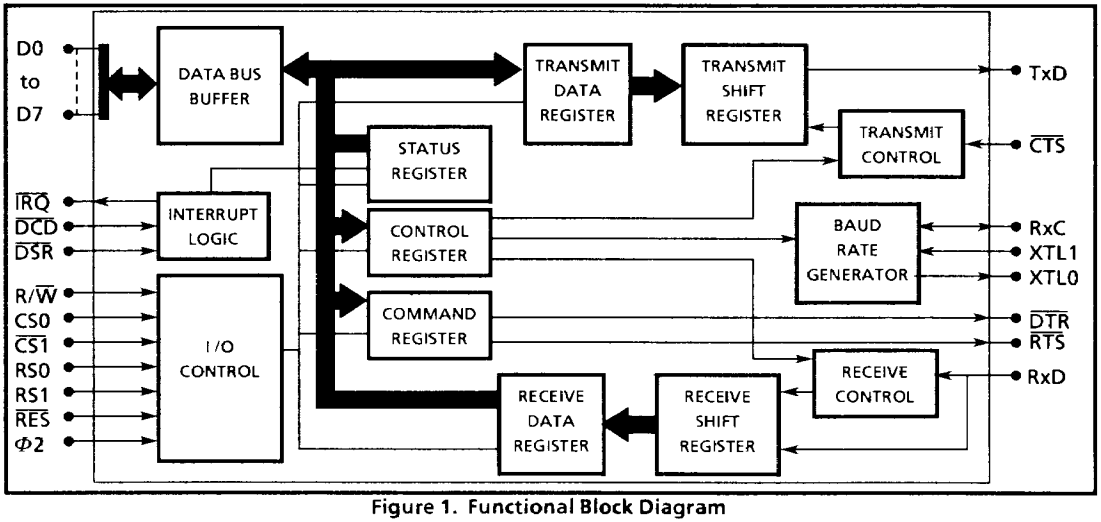


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	$V_{DD} - V_{SS}$	- 0.3	7.0	V
2	Voltage on any I/O pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current on any I/O pin	I_I		±10	mA
4	Storage Temperature	T_S	-65	+150	°C
5	Power Dissipation Plastic	P_D		0.6	W
	Ceramic	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Supply Voltage	V_{DD}	3.0	5.0	6.0	V	
2		Input Voltage	V_I	0		V_{DD}	V	
3		Operating Temperature	T_A	-40	+25	+85	°C	
4		Operating Frequency	f	0		2.0	MHz	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Quiescent Supply Current	I_{DD1}		2		µA	Outputs Unloaded
2		Operating Supply Current	I_{DD}		2		mA/MHz	Outputs Unloaded
3	I N P U T S	Input High Voltage XTAL1	V_{IH}	3.0		V_{DD}	V	
		OTHER INPUTS	V_{IH}	2.0		V_{DD}	V	
4		Input Low Voltage	V_{IL}	0		0.8	V	
5		Input Leakage Current RxC, (D_0-D_7)	I_{IZ}			10	µA	V_{IN} = 0 to V_{DD}
		Other Inputs (Except XTAL1)	I_{IZ}			2.5	µA	V_{IN} = 0 to V_{DD}
6		Input Capacitance (D_0-D_7)	C_{IN}		5.0		pF	
		Other Inputs (Except XTAL1)	C_{IN}		10.0		pF	
7		Output High Voltage (D0-7,TxD, $\overline{RTS}$, $\overline{DTR}$, RxC)	V_{OH}		V_H①		V	I_{OH} = -20 µA
			V_{OH}	2.4			V	I_{OH} = -100 µA
8		Output Low Voltage (D0-7,TxD, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$, RxC)	V_{OL}			0.4	V	I_{OL} = 1.6 mA
9		Output Leakage Current $\overline{IRQ}$ (OFF state)	I_{OZ}		10		µA	V_O = V_{SS} to V_{DD}
10		Output Capacitance	C_O		5.0		pF	

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

① $V_H = V_{DD}$ - 0.1 Volts.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes
1	MPU INTERFACE	Φ_2 Cycle Period	t_{CYC}	500	310		ns	See timing diagram 1
2		Φ_2 HIGH Pulse Width	t_C	200			ns	See timing diagram 1
3		Address Setup Time	t_{AS}	70			ns	See timing diagram 2, 3
4		Address Hold Time	t_{AH}	0			ns	See timing diagram 2, 3
5		Φ_2 to Valid Data Delay	t_{DDR}			150	ns	See timing diagram 2
6		Data Hold Time (Read)	t_{DHR}	10			ns	See timing diagram 2
7		Data Setup Time (Write)	t_{DSW}	60			ns	See timing diagram 3
8		Data Hold Time (Write)	t_{DHW}	10			ns	See timing diagram 3
9		Read/Write Setup Time	t_{RWS}	70			ns	See timing diagram 2,3
10		Read/Write Hold Time	t_{RWH}	0			ns	See timing diagram 2,3
11	COMMUNICATION INTERFACE	External TxD Clock Cycle Period	t_{ECP}	0.4			μs	See timing diagram 4
12		External TxD Clock High Duration	t_{ECH}	175			ns	See timing diagram 4
13		External TxD Clock Low Duration	t_{ECL}	175			ns	See timing diagram 4
14		External Clock to Valid Data Transmitted	t_{TXDD}			500	ns	See timing diagram 4
15		$\overline{RTS}$ and $\overline{DTR}$ Propagation Delay from Φ_2	t_{DLY}			500	ns	See timing diagram 5
16		$\overline{IRQ}$ Propagation Delay from $\Phi 2$ (CLEAR)	t_{IRQD}			500	ns	See timing diagram 5
17		External RxD Clock Cycle Period	t_{ECP}	0.4			μs	See timing diagram 6
18		External RxD Clock High Duration	t_{ECH}	175			ns	See timing diagram 6
19		External RxD Clock Low Duration	t_{ECL}	175			ns	See timing diagram 6

† Timing is over recommended temperature range & recommended power supply voltages. Test loads shown in Figures 2 and 3.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note : Rise and Fall times (t_R & t_F) are 10 to 30 ns.

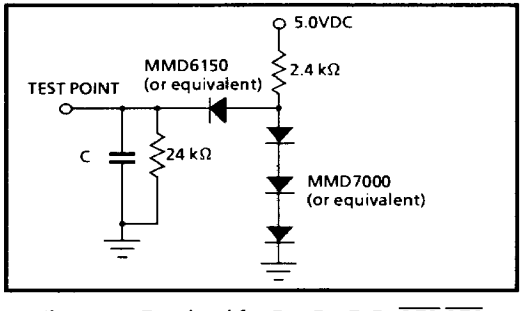


Figure 2. Test load for D_0 - D_7, TxD, $\overline{DTR}$ $\overline{RTS}$

C= 130 pF for D_0-D_7, C= 30 pF for other outputs

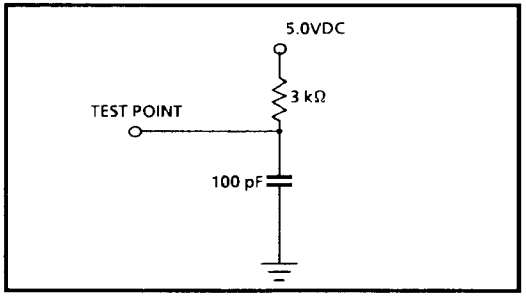
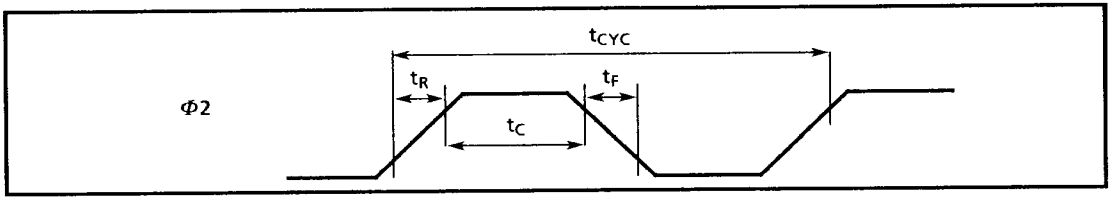


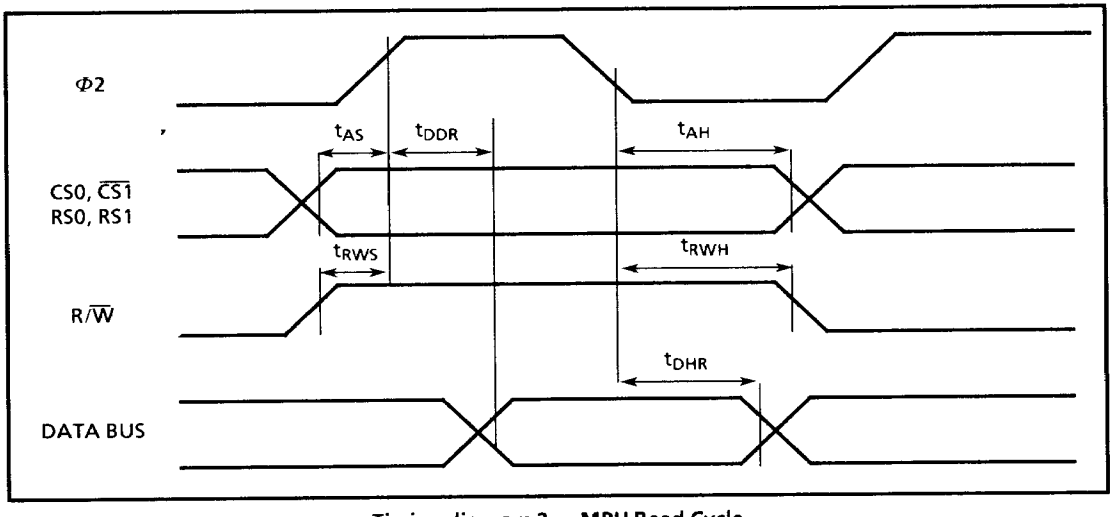
Figure 3. Test load for $\overline{IRQ}$

Timing Diagrams

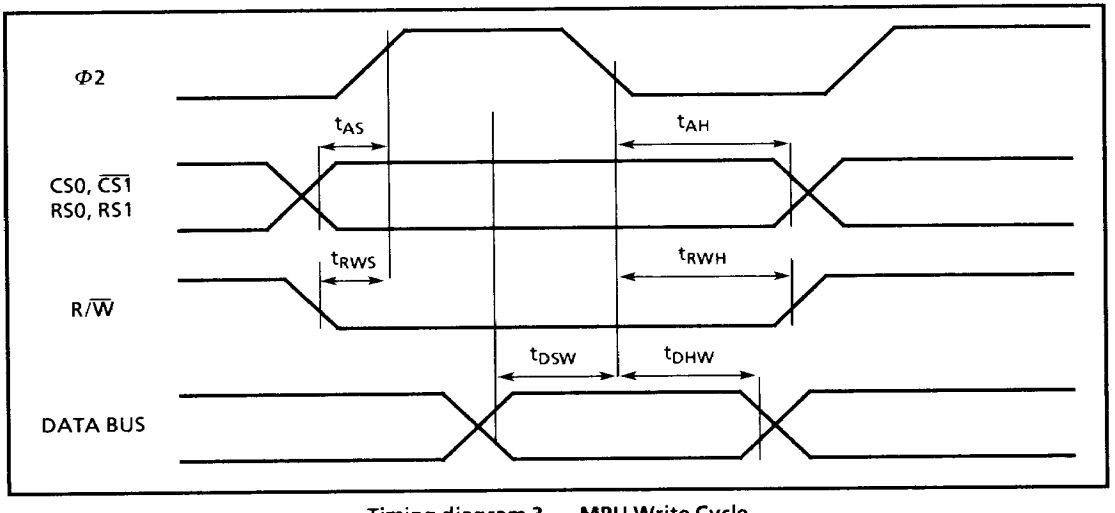
The points from which these timing values are measured are V_{IH} & V_{IL} for inputs and V_{OH} & V_{OL} for outputs.



Timing diagram 1 - Φ2 clock



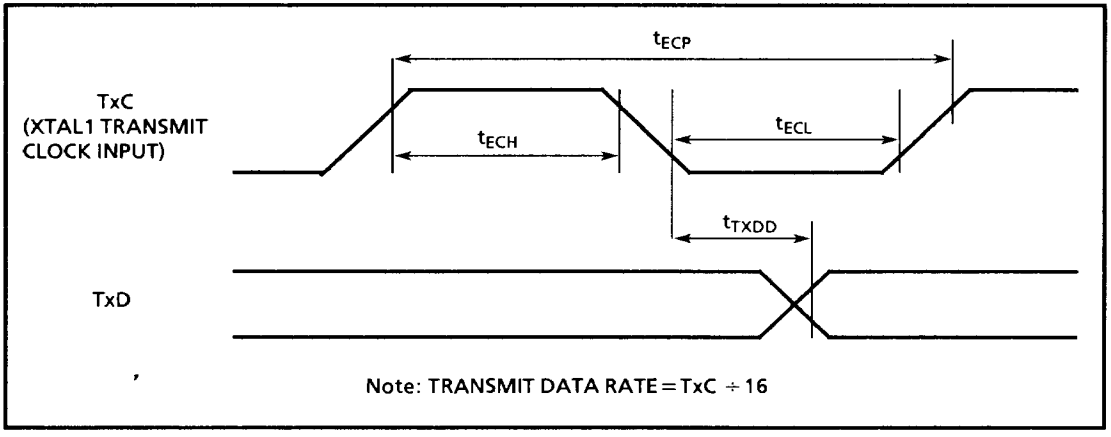
Timing diagram 2 - MPU Read Cycle



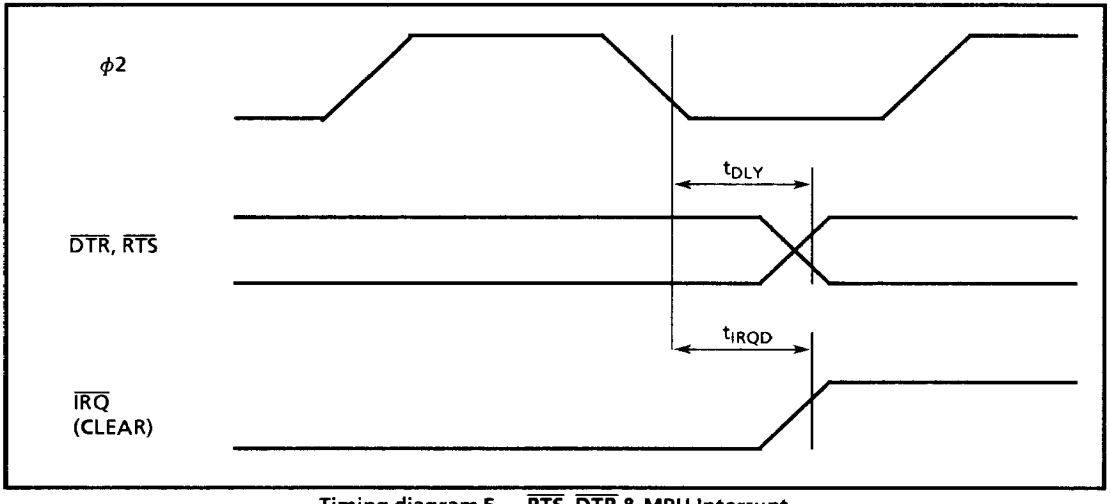
Timing diagram 3 - MPU Write Cycle

Timing Diagrams

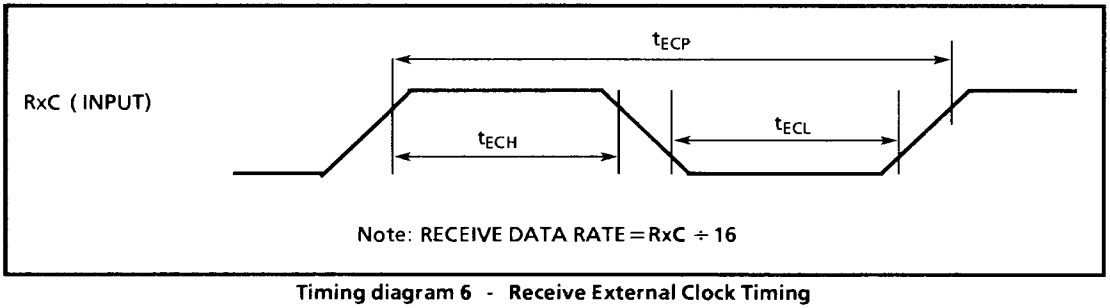
The points from which these timing values are measured are V_{IH} & V_{IL} for inputs and V_{OH} & V_{OL} for outputs.



Timing diagram 4 - Transmit Data with External Clock



Timing diagram 5 - $\overline{RTS}$, $\overline{DTR}$ & MPU Interrupt



Timing diagram 6 - Receive External Clock Timing

Pin Description

Pin	Name	Description
1	V_{SS}	**Ground Input.** 0 V.
2,3	CS0, $\overline{CS1}$	**Chip Select.** TTL inputs CS0 = 1& $\overline{CS1}$ = 0 select the chip for data transfer on the microprocessor bus. The direction of the transfer is determined by the state of the R/$\overline{W}$ pin.
4	$\overline{RES}$	**Hardware Reset.** $\overline{RES}$ = 0 to reset the chip. All internal registers will be cleared except bits 4, 5 and 6 in the Status Register (SR_b4, SR_b5 and SR_b6). SR_b4 is set, and SR_b5 and SR_b6 are unaffected.
5	RxC	**Receive Clock.** This is a bidirectional pin which serves as either the receiver 16x clock input or the receiver clock 16x output. The latter mode is selected if the internal baud rate generator is used as the receiver clock source.
6	XTAL1	**Clock Input.** For External Clock or Crystal connection. If clock is stopped, this input must be held high. XTAL1 has CMOS compatible voltage thresholds (see Figure 4).
7	XTAL0	**Clock connection.** This pin must be connected to the side of a crystal opposite to XTAL1, or left floating when using an external clock (see Figure 4).
8	$\overline{RTS}$	**Request to Send.** Output signal to the modem from the ACIA to control data transfers (see COMMAND REGISTER, Table 2).
9	$\overline{CTS}$	**Clear to Send.** Input signal from the modem to the ACIA to control data transfers. When this input is held high, the transmitter is disabled.
10	TxD	**Transmit Data.** Serial data output in NRZ (Non Return to Zero) format.
11	$\overline{DTR}$	**Data Terminal Ready.** Output to the modem to indicate the ACIA status. $\overline{DTR}$ = 1 if ACIA is disabled (see COMMAND REGISTER, Table 2).
12	RxD	**Receive Data.** Serial data input NRZ (Non Return to Zero) format.
13,14	RS0,RS1	**Register Select Inputs.** The state of these pins determines which internal register is connected to the data bus when the device is selected (see Chip Select Description and Register Decode Table).
15	V_{DD}	**Positive Supply Input.** + 5 V.
16	$\overline{DCD}$	**Data Carrier Detect Input.** Status of carrier at the modem. [$\overline{DCD}$ = 0 if the carrier is detected]. The state of this pin is reflected by bit 5 of the Status Register (SR). If interrupts are enabled (Command Register (CR) bit 0 = 1), and the logical state $\overline{DCD}$ is changed, an interrupt will occur. When not used, this input should be connected to ground or to a logic high. The input state does not affect transmitter function but a logical low must be present for the receiver to operate.
17	$\overline{DSR}$	**Data Set Ready Input.** $\overline{DSR}$ = 0 if the modem is ready to perform a data transfer. The state of this pin is reflected by SR_b6. If interrupts are enabled (CR_b0 = 1), and the logical state of $\overline{DSR}$ is changed, an interrupt will occur . When not used, this input should be connected to ground or to a logic high. The input state does not affect the transmitter or the receiver function.
18-25	D_0-D_7	**Microprocessor Data Bus.** Bidirectional data bus which is TTL compatible. When the device is not selected these pins enter a high impedance state.
26	$\overline{IRQ}$	**Interrupt Request to MPU.** (open drain output). When an interrupt occurs, this output is forced low until the interrupt is serviced (by reading the Status Register).
27	ϕ_2	**System Clock Input.** This signal synchronizes data transfers with the microprocessor.
28	R/$\overline{W}$	**Read/Write Input.** Controls the direction of data transfer between the microprocessor and the ACIA.

Functional Description

MD65SC51B Asynchronous Communications Interface Adaptor provides processor (μP) based systems with a full duplex serial interface. The μP port is directly compatible with 6800/6500 style bus architectures. Coupled with the Status Register, a powerful and flexible interrupt facility is included on the MD65SC51B to allow fast response from the μP to the ACIA.

The serial port provides signals which may be used to control a communication channel compatible to the EIA Standard RS-232C specification. An on-board baud rate generator allows 16 different baud rates, for data transmission and reception timing. All frequencies are derived from an external clock or crystal. The receive frequency may be received separately from the transmit frequency, allowing reception and transmission at independent speeds. Alternatively, the ACIA will produce a signal that is 16 times the baud rate, for use by a remote ACIA (See Pin Description - RxC).

The format of the data word is programmable. The word length ranges from five to nine bits (including parity). Parity can be odd, even or deselected altogether. The parity bit may also be forced high or low. Either 1, 1.5, or 2 stop bits may be added to the end of the serial data stream. For maintenance applications, the received data stream may be looped back onto the transmit data stream using echo mode operation.

RS1	RS0	Internal Register Selected		Reset Operation Effect															
				Hardware Reset								Programmed Reset							
		Write	Read	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	0	Transmit Data Register	Receive Data Register	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	1	Programmed Reset	Status Register	0	-	-	1	0	0	0	0	-	-	-	-	-	0	-	-
1	0	Command Register	Command Register	0	0	0	0	0	0	0	0	-	-	-	0	0	0	0	0
1	1	Control Register	Control Register	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-

Table 1 - Register Address Decoding

Note: "-" denotes no change from state previous to reset

Command Register Bit								Control Function	Resulting Function
7	6	5	4	3	2	1	0		
x	x	0	x	x	x	x	x	Parity Mode Control	No Parity Bit transmitted or received.
0	0	1	x	x	x	x	x		Odd Parity Bit transmitted or received.
0	1	1	x	x	x	x	x		Even Parity Bit transmitted or received.
1	0	1	x	x	x	x	x		Parity Bit set to MARK (Receive parity check disabled).
1	1	1	x	x	x	x	x		Parity Bit set to SPACE (Receive parity check disabled).
x	x	x	0	x	x	x	x	Echo Mode Enable	Normal Operation.
x	x	x	1	0	0	x	x		Echo Mode Enabled (bits 2 and 3 must be 0).
x	x	x	x	0	0	x	x	Transmit Interrupt Control	Transmit interrupt disabled. $\overline{RTS}$ set High (Transmitter off).
x	x	x	x	0	1	x	x		Transmit interrupt enabled. $\overline{RTS}$ set Low (Transmitter on).
x	x	x	x	1	0	x	x		Transmit interrupt disabled. $\overline{RTS}$ set Low (Transmitter on).
x	x	x	x	1	1	x	x		Transmit interrupt disabled. $\overline{RTS}$ set Low (Transmit Break on TxD).
x	x	x	x	x	x	0	x	Receiver Interrupt Enable	Receiver interrupts enabled.
x	x	x	x	x	x	1	x		Receiver interrupts disabled.
x	x	x	x	x	x	x	0	Data Terminal Ready	Data terminal not ready to transfer data ($\overline{DTR}=1$). Receiver and all interrupts disabled.
x	x	x	x	x	x	x	1		Data terminal ready to transfer data ($\overline{DTR}=0$). Receiver and all interrupts enabled.

Table 2 - Command Register Description

Note: "x" is intended to represent don't care in all binary representations in this and all following tables.

Serial Interface Description

Transmitted and Received Data

Data is transmitted from the ACIA on the TxD pin, and received on the RxD pin. The inactive state of either data channel (RxD or TxD) is a mark condition (logical high). This type of data code is termed Non-Return to Zero (NRZ). Data transmitted or received by the MD65SC51B is always preceded by a "start bit".

The start bit is a space condition (logical low) which signifies the start of active data on the channel. The receiving ACIA also uses the start bit to optimize its sampling for the middle of the data bits that follow. Between received words, the ACIA samples the channel at 16x Baud rate. When a low is detected, the ACIA waits half a bit period before sampling again. This delay allows subsequent bits (sampled at the same frequency as the baud rate) to be sampled as far from the bit boundaries as possible. Noise or "glitch" immunity is also added by this mechanism. Low going pulses of less than 1/2 a bit period wide will not be mistaken for the start bit (the ACIA resumes the 16x sampling rate).

Data bits following the start bit are in ascending order, with the least significant bit (LSB) first, and the most significant bit (MSB) last. The MSB depends on the number of bits per word selected; the ACIA can be programmed for 5 bit, 6 bit, 7 bit or 8 bit data word transmission/reception. Each bit has a period equal to the reciprocal of the selected baud rate, which in turn is dependent on the clock source frequency (see Table 4).

Parity sensing and generation can be chosen for odd parity, even parity or no parity. When parity is selected, the parity bit follows the MSB of the data word. For even parity, the condition of the parity bit will be such that there are an even number of

Control Register Bit								Control Function	Resulting Function
7	6	5	4	3	2	1	0		
0	x	x	x	x	x	x	x	Stop Bit Control	1 stop bit.
1	x	x	x	x	x	x	x		2 stop bits except in the following cases: a/ 1 stop bit if word length set for 8 bits & parity enabled ② b/ 1.5 stop bits if word length set for 5 bits & parity disabled
x	0	0	x	x	x	x	x	Word Length Setting	8 bits
x	0	1	x	x	x	x	x		7 bits.
x	1	0	x	x	x	x	x		6 bits.
x	1	1	x	x	x	x	x		5 bits.
x	x	x	0	x	x	x	x	Receiver Clock Source	External clock source. (RxC is Input)
x	x	x	1	x	x	x	x		Internal baud rate generator. (RxC is Output)
x	x	x	x	0	0	0	0	Baud Rate Control	115.2 kbaud① or (Frequency) ÷ 16
x	x	x	x	0	0	0	1		50 baud① or (Frequency) ÷ 36,864
x	x	x	x	0	0	1	0		75 baud① or (Frequency) ÷ 25,576
x	x	x	x	0	0	1	1		109.92 baud① or (Frequency) ÷ 16,769
x	x	x	x	0	1	0	0		134.58 baud① or (Frequency) ÷ 13,704
x	x	x	x	0	1	0	1		150 baud① or (Frequency) ÷ 12,288
x	x	x	x	0	1	1	0		300 baud① or (Frequency) ÷ 6,144
x	x	x	x	0	1	1	1		600 baud① or (Frequency) ÷ 3,072
x	x	x	x	1	0	0	0		1200 baud① or (Frequency) ÷ 1,536
x	x	x	x	1	0	0	1		1800 baud① or (Frequency) ÷ 1,024
x	x	x	x	1	0	1	0		2400 baud① or (Frequency) ÷ 768
x	x	x	x	1	0	1	1		3600 baud① or (Frequency) ÷ 512
x	x	x	x	1	1	0	0		4800 baud① or (Frequency) ÷ 384
x	x	x	x	1	1	0	1		7200 baud① or (Frequency) ÷ 256
x	x	x	x	1	1	1	0		9600 baud① or (Frequency) ÷ 192
x	x	x	x	1	1	1	1		19.2 kbaud① or (Frequency) ÷ 96

Table 4 - Control Register Description

Notes : ① The preset baud rates given assume a crystal frequency of 1.8432 MHz
② To enable and disable parity, see Table 2.

marks when considering the data word and the parity bit. With odd parity, the condition of the parity bit will be such that there is an odd number of marks when considering the data word and the parity bit (both cases exclude the start and stop bits).

Transmit and Receive Clocks

The signals used by the ACIA for transmit/receive timing are found on three pins: XTAL0, XTAL1 and RxC. XTAL1 and XTAL0 are the input and output, respectively, of a crystal oscillator circuit. The crystal can be connected to these pins as seen in Figure 4. This oscillator circuit drives the internal baud rate generator, which divides the squarewave output of the oscillator by the divisor selected (see Table 4). If a crystal is not used, an external clock may drive the oscillator input while the oscillator output is left floating. If the clock is stopped (device still powered), the oscillator input should be held to a logical high.

The clock for the receiver may be taken from one of two sources: the output of the internal baud rate generator, or from an external clock input on the RxC pin. In the latter case, the baud rate is 1/16th of the external clock. If the source of receiver timing is the internal baud rate generator, RxC becomes an output and sources a clock 16 times (16x) the baud rate (for driving remote ACIAs).

Control Signals

These signals are compatible with the RS-232C modem control circuits. The signals are the Request To Send ($\overline{RTS}$), Data Terminal Ready

Characteristics	Spec.
Temperature stability @ -45 to +85°C	±0.01%
Frequency* (MHz)	1.8432
Frequency tolerance* (±%)	0.02
Resonance mode*	parallel
Equivalent resistance* (ohms)	400 max.
Drive level* (mW)	2
Shunt capacitance* (pF)	7 max.
Load capacitance* (pF)	16.5 typ.
Oscillation mode*	Funda-mental

Table 6 - Crystal Specification

*characteristics at 25°C± 2°C

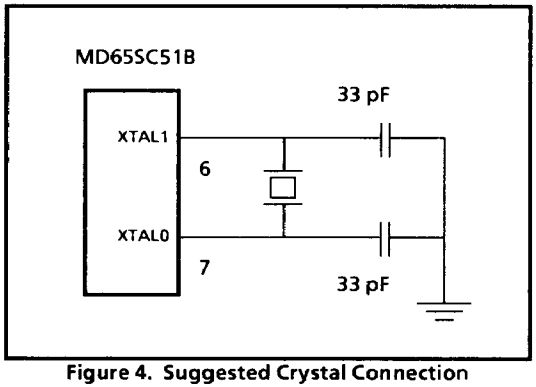


Figure 4. Suggested Crystal Connection

Status Register bit	Control Signal	Status Flag Set by	Status Flag Cleared by
0	PARITY ERROR③	Parity error detected.	Cleared Automatically after a read of the Receive Data Register and next error free reception of data.
1	FRAMING ERROR③	Framing error detected.	
2	OVERRUN③	Overrun has occurred.	
3	RECEIVE REGISTER	Register full.	Read Receive Data Register
4	TRANSMIT REGISTER	Register empty.	Write Transmit Data Register.
5	$\overline{DCD}$	Carrier not detected (a high on $\overline{DCD}$).④	Carrier detected (a low on $\overline{DCD}$).④
6	$\overline{DSR}$	Data set not ready (a high on $\overline{DSR}$).④	Data set ready (a low on $\overline{DSR}$).④
7	INTERRUPT	Interrupt has occurred. The $\overline{IRQ}$ signal to the microprocessor also goes low.	Read Status Register. This also clears the $\overline{IRQ}$ signal to the microprocessor.

Table 5 - Status Register Description

Notes ③ No interrupt is generated from these conditions.
④ These bits are not resetable and reflect the state of the input.

($\overline{DTR}$) outputs and the Clear To Send ($\overline{CTS}$), Data Set Ready (DSR) and Data Carrier Detect ($\overline{DCD}$) inputs. Note that the ACIA is viewed as the Data Termination Equipment (DTE) as opposed to the Data Communication Equipment (DCE) when referencing the RS-232C specification.

Request To Send. $\overline{RTS}$ is used to indicate to the DCE that it should assume the data channel transmit mode. The state of this output is controlled by bits 2 and 3 of the Command Register ($COMR_b2$ and $COMR_b3$, see Table 2). When it is high (not asserted, or in other words, "negated") the ACIA's transmitter is disabled.

Data Terminal Ready. The $\overline{DTR}$ signal indicates to the DCE that the ACIA is ready for communication. This output is asserted when $COMR_b0$ is set.

Clear To Send. The $\overline{CTS}$ signal from the DCE tells the ACIA that the DCE is prepared to accept data to pass on to the remote end of the communication channel. When this signal is not asserted, the transmitter of the ACIA is disabled. If the ACIA is in the middle of transmitting a data word when $\overline{CTS}$ is negated, the TxD channel goes immediately to a mark condition. The data word being transmitted at the time is lost, but the character (if any) in the Transmit Data Register (TDR) is not (see register description). As soon as $\overline{CTS}$ is asserted, this dataword will be transmitted, if the transmitter is still enabled internally (see Figure 8).

Data Set Ready. The $\overline{DSR}$ signal from the DCE tells the ACIA that the DCE is ready to operate. A transition on this pin can cause an interrupt (if interrupts are enabled) and the state of the pin is reflected in the state of SR_b6. Transitions that follow will not affect the status bit until after the µP has serviced the first interrupt (read the SR). At that point the SR will again reflect the current level of the $\overline{DSR}$ input, and an interrupt will occur again if it has changed. Transmitter and receiver operation is not affected by the level of this pin.

Data Carrier Detect. The $\overline{DCD}$ signal from the DCE indicates to the ACIA that the received signal is within specified limits. When $\overline{DCD}$ is not true, the receiver of the ACIA will be disabled and the data being shifted in at that moment is lost. A transition on this pin, like the $\overline{DSR}$ input, causes an interrupt. Subsequent transitions will not affect the status bit until the first interrupt is serviced. If the pin has changed since the first occurred and before it was serviced, another interrupt will occur. An even number of level changes on $\overline{DSR}$ and $\overline{DCD}$, before the first interrupt has been serviced, will not cause another interrupt. This is because the status bits will be at the same logic level that caused the original interrupt.

Register Description

The MD65SC51B contains seven registers, five that are visible to the µP. These registers are: the Transmit Shift Register (TSR, not available toµ P), the Receive Shift Register (RSR, not available to µP), the Transmit Data Register (TDR), the Receive Data Register (RDR), the Status Register (SR), the Command Register (COMR), and the Control Register (CR). One of the five latter registers is visible to the µP when the chip selects (CS0, CS1) are asserted and the E clock is true (high); the register chosen by the state of the register selects (RS0, RS1). The direction of µP bus transfer is determined by the state of the R/$\overline{W}$ signal (a high indicates a read of the contents of the register, a low a write to a register). When the SR is written to (the data written doesn't matter) a software reset will occur. For a comparison between the effect of a hardware reset and a software reset, see Table 1.

Transmit Data Register

The Transmit Data Register (TDR), in conjunction with the Transmit Shift Register, is used to place data on the transmit channel (TxD). If no word is being transmitted, a data word written to the TDR is immediately transferred into the TSR to be shifted out. A start bit precedes the data on the TxD channel; parity is added to the end of the word as needed (after the valid MSB is shifted out); and 1, 1.5, or 2 stop bits follow to end the transmitted information. If the ACIA is programmed to send a data word that is less than 8 bits in length (5, 6 or 7 bits), the extra bits in the data word are ignored.

While the TSR is occupied shifting out active data on to TxD (including the bit periods for the transmission of parity bits and stop bits), information written to TDR will be latched and held. When the last stop bit of the previous word is finished, the ACIA will transfer the data word in the TDR into the TSR and transmit it. If the TDR is written to more than once while information is being transmitted on TxD, the data word in TDR will be overwritten and retain the data associated with the last write.

If transmit interrupts are enabled, when the TDR is empty an interrupt will occur and SR_b4 will be set (SR_b4 will be set even if interrupts are disabled). This coincides with the beginning of the start bit for the data just transferred to the TSR. The interrupt must be serviced to be removed (by reading SR), but SR_b4 may only be cleared by a write to the TDR. If the interrupt is serviced but TDR is not written to,

another interrupt will occur at the next word boundary (word boundaries are referenced to the start of the last transmitted word, and occur every full word period after the end of that word. This timing is reset by a new transmission because, if TxD is idle the new word is transmitted immediately - see Figures 5 & 7.

Receive Data Register

Data on the receive channel (RxD) is stripped of the overhead bits (start, parity and stop) by the ACIA and shifted into the Receive Shift Register (RSR). When a full data word has been received (depending on the programmed length), the contents of the RSR are transferred into the Receive Data Register (RDR). If receive interrupts are

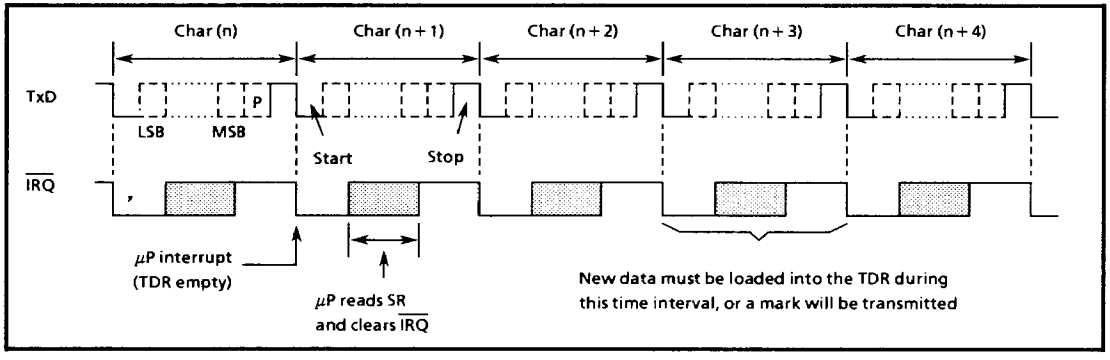


Figure 5. Continuous Data Transmit

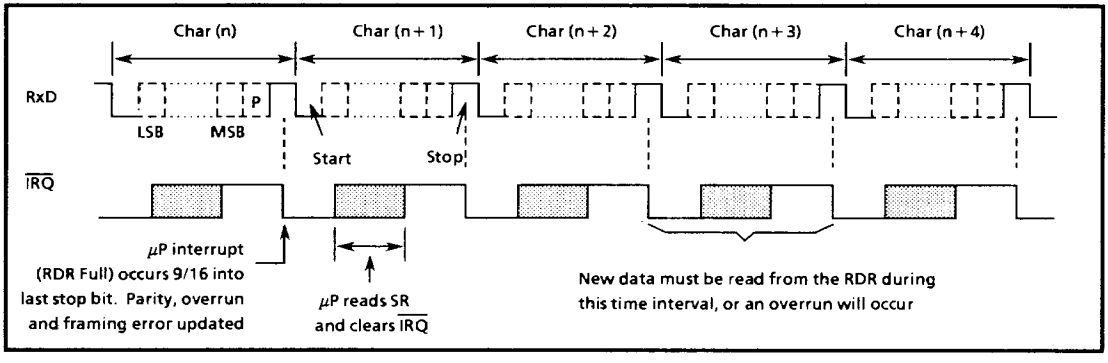


Figure 6. Continuous Data Receive

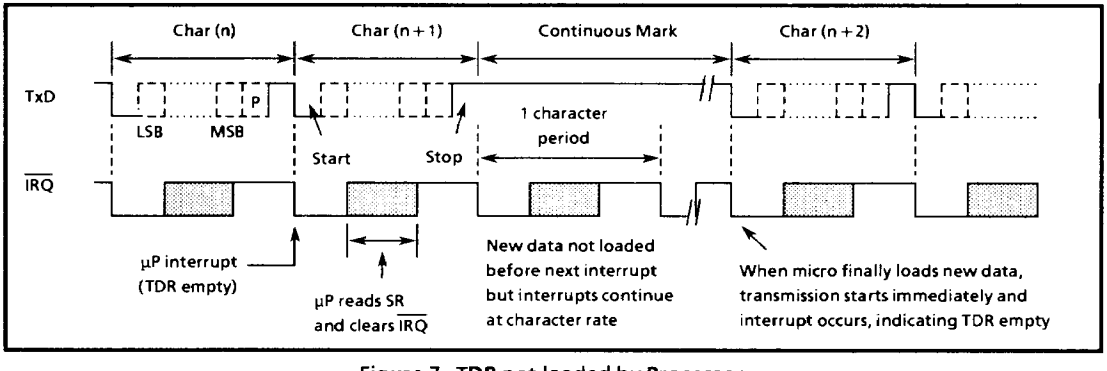


Figure 7. TDR not loaded by Processor

enabled, this transfer will cause an interrupt to occur and SR_b3 to be set (SR_b3 is set even when interrupts are disabled). The interrupt actually occurs about 9/16 through the last stop bit. As with the TDR, the interrupt is removed by reading SR and SR_b3 is cleared by reading the RDR.

If $\overline{DCD}$ is not asserted, the RSR is immediately disabled and any word being received at the time is lost. If the receive circuitry is disabled through the Command Register, a data word in the process of being received will be finished before the the RSR is disabled.

When a continuous break character is received, the first character period will look like a data word of all zeros and a framing error. If interrupts are enabled, an interrupt will occur. Thereafter the receiver will be disabled until a stop bit is received, so no more interrupts will occur. It is possible that the μP could interpret a data word made up of zeros, without a stop bit in the correct position, as a received break condition (see Figures 6 and 12).

Command Register

The Command Register (COMR) determines the type of parity used in the transmitted word, and the type of parity checked for in the received word. Parity is controlled by COM_b5 - COM_b7 (see Table 2). The bit position normally occupied by a parity bit may be forced to a mark or a space if required.

$COMR_b4$ enables or disables echo mode (for echo to be enabled, COM_b2 and COM_b3 must both be 0). When in echo mode, the ACIA's receive circuitry is still operational, but data written to the TDR will not be transmitted until echo mode is disabled and the transmitter is re-enabled. $\overline{RTS}$ is asserted in echo mode, even though it is not programmed to be active by $COMR_b3$ and $COMR_b2$.

When data is received on RxD (the receiver must be enabled internally and $\overline{DCD}$ true) it is transmitted 1/2 bit period after it has been received. Interrupts occur just as they would when initiated by any received data (If interrupts are enabled). If echo mode is disabled during reception of a character, transmission on TxD stops immediately and $\overline{RTS}$ is negated. The word continues to be shifted into the RSR if it is still enabled (see Figures 10 and 11).

$COMR_b2$ and $COMR_b3$ control the transmit circuitry, disabling or enabling the transmitter and $\overline{RTS}$, and disabling or enabling transmit interrupts. If continuous break mode is selected during the transmission of a data word, the current word will be transmitted and the break condition will begin immediately after. Transmit interrupts are automatically disabled during the transmit break condition.

The break condition will last for at least one character period, so if the transmitter is enabled immediately after the break condition has been set (assuming the ACIA has begun to transmit the break) the transmitter will not return to normal operation until after one character period of break.

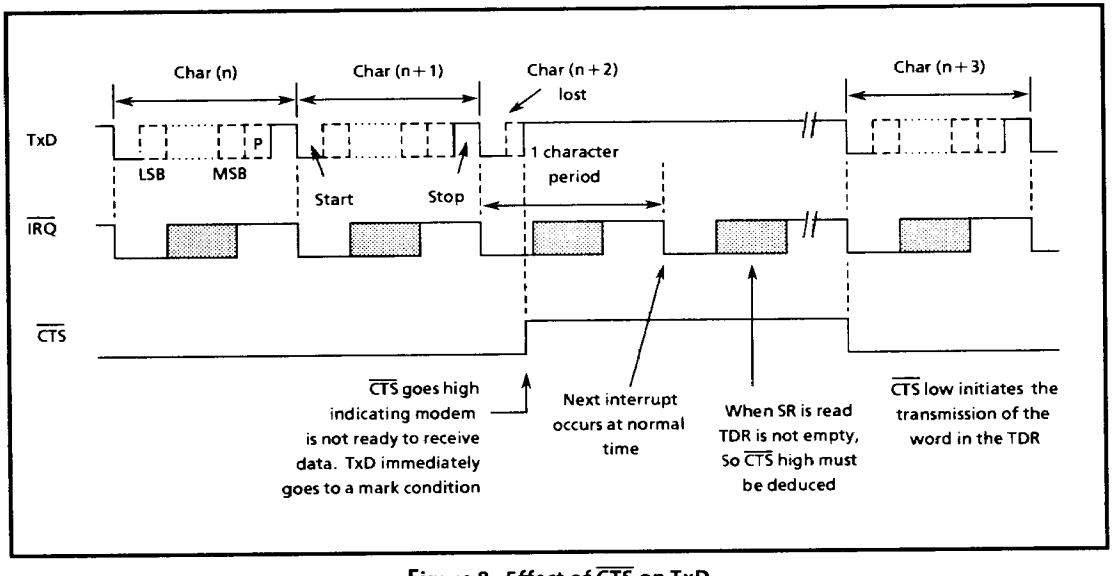


Figure 8. Effect of $\overline{CTS}$ on TxD

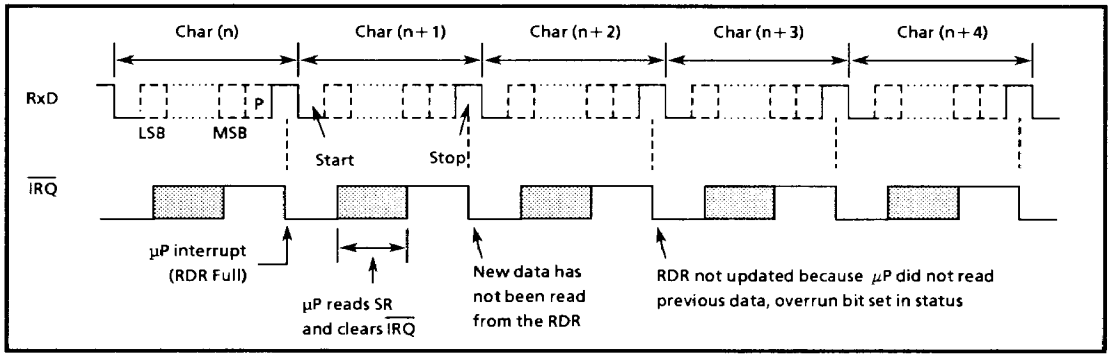


Figure 9. Effect of Overrun on Receiver

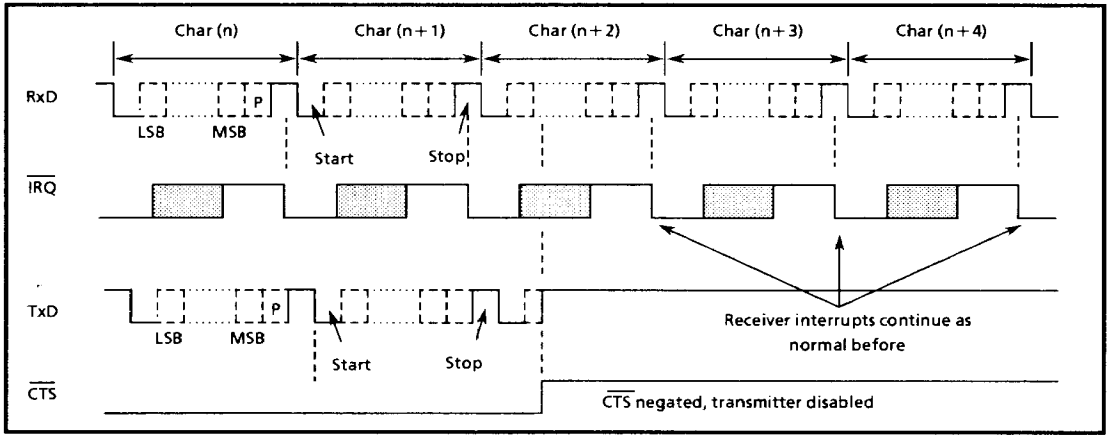


Figure10. Effect of $\overline{CTS}$ on Echo Mode operation

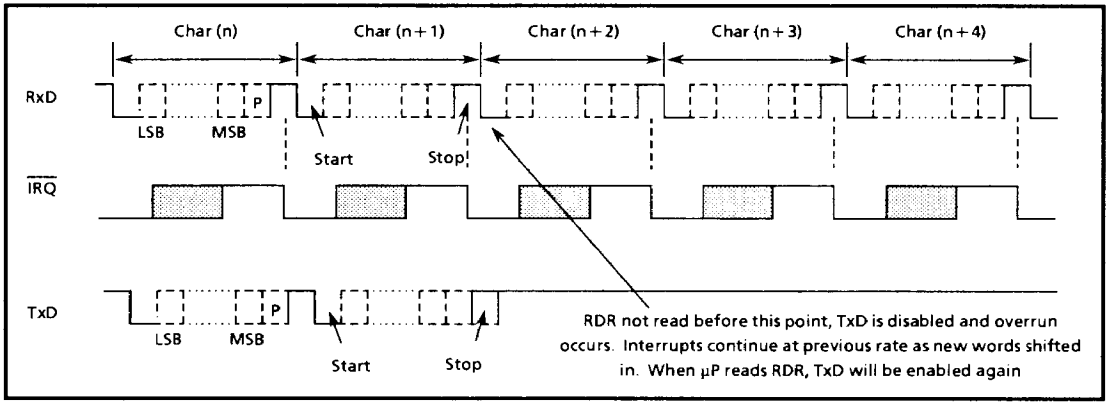


Figure 11. Overrun in Echo Mode

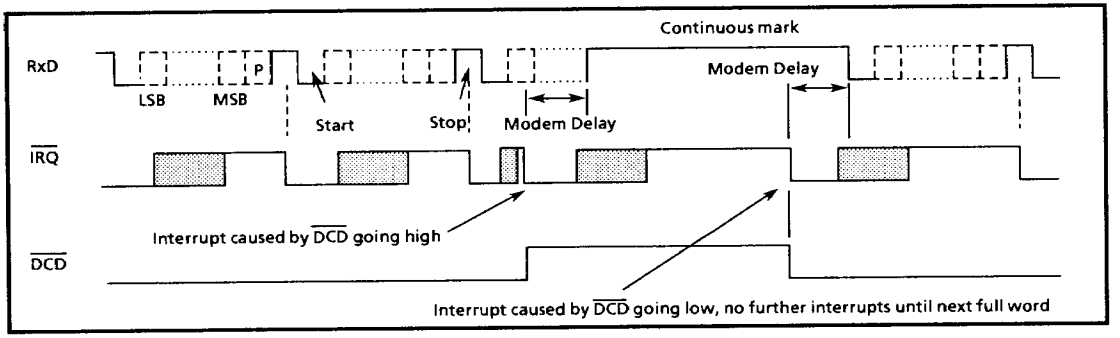


Figure12. Effect of $\overline{DCD}$ on Receiver

When the break mode is removed, one stop bit will be placed on TxD before the transmission of the next word.

$COMR_b1$ enables or disables receiver interrupts and $COMR_b0$ enables or disables the receiver circuitry, all interrupts and the $\overline{DTR}$ signal. See Figure 3.

Control Register

The Control Register (CR) determines the number of stop bits in transmitted and received information; the length of the word: the source of the receive and transmit timing and the divisor used by the baud rate generator.

Note that when the receiver clock source is chosen such that RxC is an input, the setting of the baud rate generator has no effect on the receiver speed. See Table 3.

Status Register

The Status Register (SR) performs a "housekeeping" function for the ACIA. The SR contains several error bits, two bits to display the state of the transmit and receive registers, two bits used for modem status and one bit for displaying interrupt status. SR_b7 is the inverse of the $\overline{IRQ}$ signal. When an interrupt is active, SRb7 is set. It is cleared by reading the SR,

SR_b5 and SR_b6 reflect the state of the $\overline{DCD}$ pin and the $\overline{DSR}$ pin respectively. These bits cannot be reset or cleared by the µP.

SR_b3 is the Receive Data Register full bit and SR_b4 is the Transmit Data Register Empty bit. These bits have been described fully in the TDR and RDR sections.

The three LSB bits in the SR are error bits, set when a specific error condition occurs. These bits may only be cleared if the RDR is read and a word is received without an error (the error that occurred previously). SR_b0 is the parity error detect bit. When this bit is set, it indicates that parity is enabled and the level of the parity bit received by the ACIA was incorrect. SR_b1 is the framing error detect bit. If a word is received that does not have a stop bit where expected, the framing error bit will be set.

SR_b2 is the overrun error bit. This bit is set if a data word is received without the previous word having been read. The word in the RDR is maintained until it is read, so subsequent words in the RSR, that result in an overrun condition, are lost. Interrupts continue to occur with each data word received in the RSR as normal (see Figure 9). When an overrun occurs in echo mode, the TxD channel goes to a mark until the first start bit after the RDR is read by the µP.

Suggested sequence for reading SR after interrupt:

1/ *Read Status Register.*
This operation automatically clears SR_b7 and negates the IRQ signal. Subsequent transitions on DSR and DCD will cause another interrupt.
2/ *Check SR_b7*
If not set, source was not the ACIA.
3/ *Check SR_b6 and SR_b5*
These must be compared to their previous levels, which must be stored externally by the processor. If they are both a logical low (modem on-line) and they are unchanged then the remaining bits must be checked.
4/ *Check SR_b3*
Is RDR full?
5/ *Check SRb0, SRb1, SRb2*
Only if RDR is set.
6/ *Check SR_b4*
Is TDR empty? Check even if RDR is full when in full duplex operation.
7/ If none of the above occurred, $\overline{CTS}$ must have been negated.

MD65SC51B ACIA Improvements

The MD65SC51B Asynchronous Communications Interface Adapter is a popular design, sourced by many manufacturers. However, many of the CMOS versions of the 6551 ACIA originate from a common design source and may present some intermittent problems. The problems may be summarized as follows:

a) In "noisy" environments, the baud rate generator could lock up, inhibiting transmission and/or reception.

b) The start bit of a character would occasionally be shorter than it should have been for a particular baud rate setting.

c) Information being transmitted could be overwritten by information meant for the Transmit Register. Correct operation would latch the new information while finishing the transmission of the old.

d) The parity bit would occasionally be set when it should have been cleared.

The first problem may occur when noise sets the programmable baud rate generator logic array into a disallowed state. The solution was to detect this state and upon detection, leave the state immediately.

The last three problems are the result of sensitivity of internal asynchronous signals to CMOS process variations. Mitel eliminated these problems completely in the MD65SC51B by appending a mark state, 1/16th of a bit period in width, to the last stop bit of each transmitted character. This extra mark time may affect device operation in instances where the total bandwidth of the ACIA transmit channel is used. In such a case, if the ACIA is set up to transmit characters that are for example, 10 bits in length (including start, stop and parity bits), the maximum throughput of the ACIA on the transmit side will be decreased by 0.625%. In normal applications, this decrease in throughput would be offset by transmitter inactive time, where the ACIA is not transmitting anything.

The addition of 1/16th of a bit to each character also causes two formerly simultaneous transmit interrupts to be separated by 1/16th of a bit. This separation of the interrupts can only be seen if the microprocessor controlling the ACIA services the first interrupt within the 1/16th of a bit time. Figure 13 shows the relationship between TxD, $\overline{IRQ}$ and the added 1/16th mark state.

The transmit interrupts are caused by the end of the stop bit of the last transmitted character and the falling edge of the start bit of the next character being transmitted. The second interrupt is a potential problem, because the status register does not indicate that the transmit register is empty if it was written to when servicing the first interrupt (this is logical because the register is not empty). This condition looks like the ACIA just had its $\overline{CTS}$ input negated while transmitting one character with another in the transmit register. This is only a problem if $\overline{CTS}$ is being used in flow control applications. The problem can be solved if $\overline{CTS}$ is tied to the $\overline{DCD}$ input or the $\overline{DSR}$ input, giving $\overline{CTS}$ visibility in the status register.

The occurrence of the two interrupt condition is obviously affected by the speed of the microprocessor and the programmed baud rate. Decreasing the microprocessor interrupt service routine execution speed or increasing the programmed baud rate of the ACIA decreases the chances of servicing the first interrupt within 1/16th of a bit.

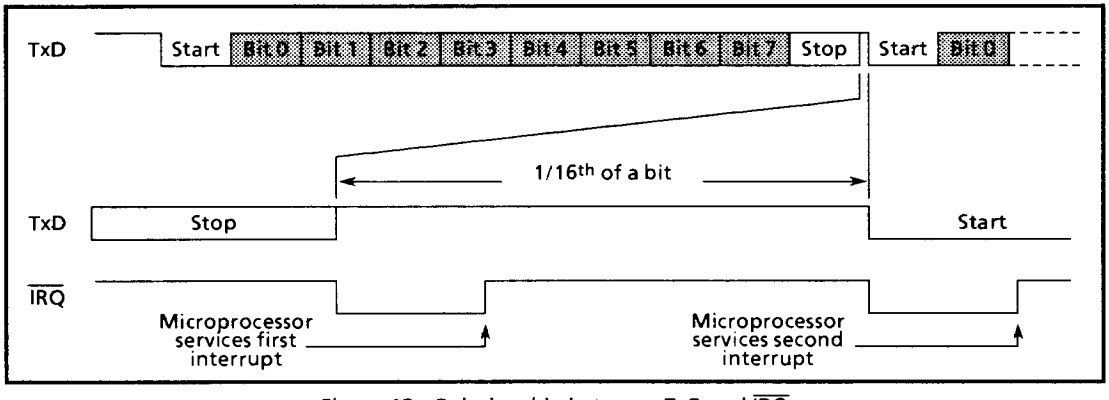


Figure 13 - Relationship between TxD and $\overline{IRQ}$