APPLICATION NOTE

AP-370

82557

LAN Design Guide

10/100 Mbps Ethernet* LAN Designs Using the Intel 82557

Version 2.2

Technical Marketing

Network Products Division

Intel Corporation

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CONTENTS

1. INTRODUCTION

This application note provides information on how to implement 10BASE-T and 100BASE-T LAN designs using the Intel 82557 PCI LAN Controller. Included are helpful guidelines and reference design information used to assist the designer in developing various Ethernet designs using the 82557.

Note:
This document contains information on various devices other than Intel which are designed to work with the 82557. For additional details on these devices, please refer to the specific vendor of that component.

2. 82557 OVERVIEW

2.1 82557 Description

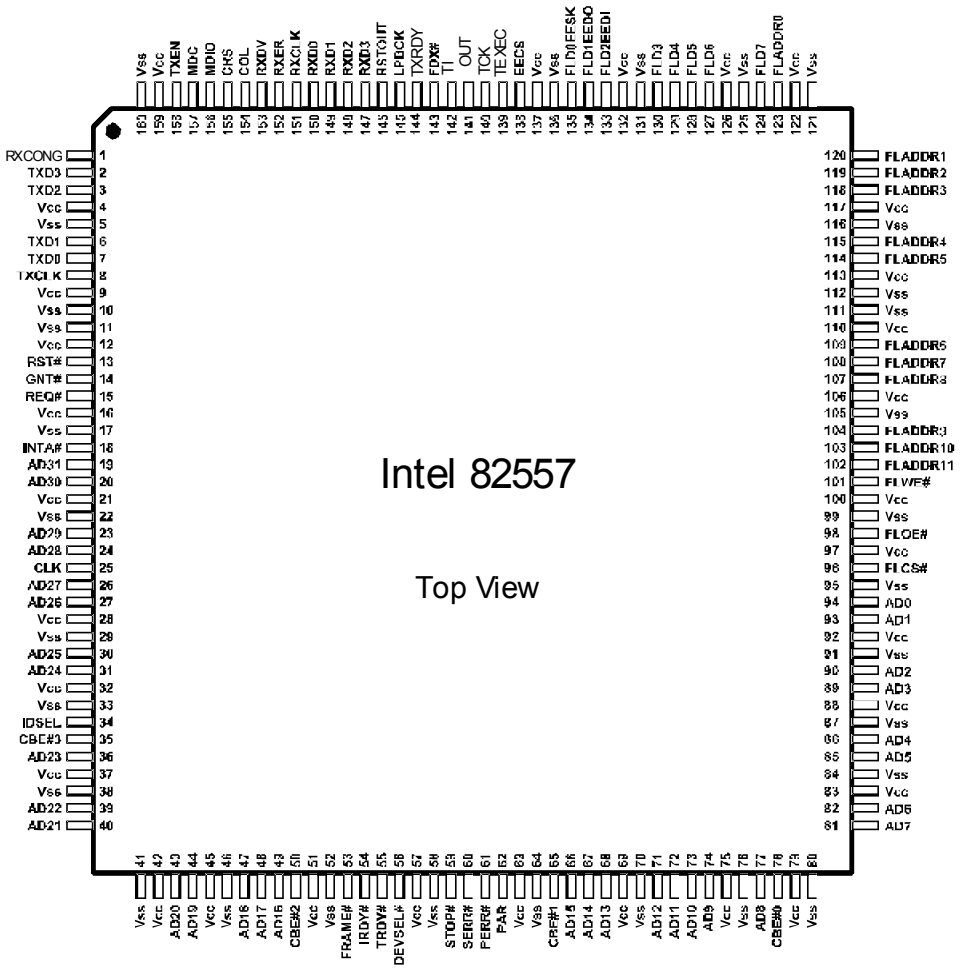
The 82557 is Intel's first highly integrated 32-bit PCI LAN controller for 10/100 Mbps Ethernet networks. It provides compatibility with ANSI/IEEE Standard 802.3/802.3u, which includes 10BASE-T and 100BASE-T specifications. It contains a high-performance 4-Channel DMA, 32-bit PCI Bus Master Interface to fully utilize the PCI's high bus bandwidth (up to 132 Mbytes per second). This allows the 82557 to deliver maximum throughput while maintaining as low CPU utilization as possible.

The 82557 contains two 3 Kbyte receive and transmit FIFOs, which prevent data overruns or underruns while waiting to access the PCI bus. In addition, the 82557 performs back to back frame transmission within the minimum interframe spacing. The 82557 includes a glueless EEPROM interface for node address and vendor specific storage information. Full support for up to 1 Mbyte of FLASH enables remote boot capability (a BIOS extension stored in the FLASH which could allow a node to boot itself off of a network drive). For 100 Mbps applications, the 82557 contains an IEEE MII compliant interface to any MII compliant 100BASE-TX or 100BASE-T4 PHY. For 10 Mbps networks, the 82557 can interface with a standard ENDEC device (such as the Intel 82503 Serial interface), while maintaining software compatibility with 100 Mbps solutions.

The 82557 is designed to implement cost effective, high performance PCI add-in adapters, PCI LAN on motherboards, or other interconnect devices including switches or bridges. Its combination of high integration and low cost make it ideal for these applications.

The figure on the next page shows the 82557 pin out information.

Note:
For additional information on the 82557, consult the 82557 Data Sheet and 82557 User's Manual, available from your local Intel Sales Representative.


Intel 82557
Top View
RXCONG 1
TXD3 2
TXD2 3
Vcc 4
Vss 5
TXD1 6
TXD0 7
TXCLK 8
Vcc 9
Vss 10
Vss 11
Vcc 12
RST# 13
GNT# 14
REQ# 15
Vcc 16
Vss 17
INTA# 18
AD31 19
AD30 20
Vcc 21
Vss 22
AD29 23
AD28 24
CLK 25
AD27 26
AD26 27
Vcc 28
Vss 29
AD25 30
AD24 31
Vcc 32
Vss 33
IDSEL 34
CBE#3 35
AD23 36
Vcc 37
Vss 38
AD22 39
AD21 40
Vss 41
Vcc 42
AD20 43
AD19 44
Vcc 45
Vss 46
AD18 47
AD17 48
AD16 49
CBE#2 50
Vcc 51
Vss 52
FRAME# 53
IRDY# 54
TRDY# 55
DEVSEL# 56
Vcc 57
Vss 58
STOP# 59
SERR# 60
PERR# 61
PAR 62
Vcc 63
Vss 64
CBE#1 65
AD15 66
AD14 67
AD13 68
Vcc 69
Vss 70
AD12 71
AD11 72
AD10 73
AD9 74
Vcc 75
Vss 76
AD8 77
CBE#0 78
Vcc 79
Vss 80
Vss 160
Vcc 159
TXEN 158
MDC 157
MDIO 156
CRS 155
COL 154
RXDV 153
RXER 152
RXCLK 151
RXD0 150
RXD1 149
RXD2 148
RXD3 147
RSTOUT 145
LPBCK 145
TXRDY 144
FDX# 143
TI 142
OUT 141
TCK 140
TEXEC 139
EECS 138
Vcc 137
Vss 136
FLD0EESK 135
FLD1EEDO 134
FLD2EEDI 133
Vcc 132
Vss 131
FLD3 130
FLD4 129
FLD5 128
FLD6 127
Vcc 126
Vss 125
FLD7 124
FLADDR0 123
Vcc 122
Vss 121
FLADDR1 120
FLADDR2 119
FLADDR3 118
Vcc 117
Vss 116
FLADDR4 115
FLADDR5 114
Vcc 113
Vss 112
Vss 111
Vcc 110
FLADDR6 109
FLADDR7 108
FLADDR8 107
Vcc 106
Vss 105
FLADDR9 104
FLADDR10 103
FLADDR11 102
FLWE# 101
Vcc 100
Vss 99
FLOE# 98
Vcc 97
FLCS# 96
Vss 95
AD0 94
AD1 93
Vcc 92
Vss 91
AD2 90
AD3 89
Vcc 88
Vss 87
AD4 86
AD5 85
Vss 84
Vcc 83
AD6 82
AD7 81

2.1.1 82557 Parallel Interface

The 82557 Parallel Interface consists of the PCI Bus interface and the Local Memory Interface. The following table summarizes the parallel signals and pins.

Signal Grouping	Signal Name	Corresponding Signal Pin Number
PCI Interface		
	Address / Data (AD0-31)	94, 93, 90, 89, 86, 85, 82, 81, 77, 74, 73, 72, 71, 68, 67, 66, 49, 48, 47, 43, 44, 40, 39, 36, 31, 30, 27, 26, 24, 23, 20, 19
	Bus Command and Byte Enables (CBE#0-3)	78, 65, 50, 35
	Parity (PAR, SERR#, PERR#)	62, 60, 61
	Interface Control (FRAME#, IRDY#, TRDY#, STOP#, IDSEL#, DEVSEL#)	53, 54, 55, 59, 34, 56
	Interrupt (INTA#)	18
	Arbitration (REQ#, GNT#)	15, 14
	System (CLK, RST#)	25, 13
Local Memory Interface		
	EEPROM (EECS, FLF0EESK, FLD1EEDO, FLD2EEDI)	138, 135, 134, 133
	FLASH (FLF0EESK, FLD1EEDO, FLD2EED1, FLD3-7, FLADDR0-11, FLCS#, FLOE#, FLWE#)	135, 134, 133, 130, 129, 128, 127, 124, 123, 120, 119, 118, 115, 114, 109, 108, 107, 104, 103, 102, 96, 98, 101

2.1.1.1 PCI Interface

The glueless PCI interface connects to the PCI bus and provides control, address, and data information to and from the host. The 82557 operates as both a master and slave on the PCI bus. As a master, the 82557 interacts with the system memory to access data for transmission, or receive data for reception. As a slave, some 82557 control structures are accessed by the host CPU, which reads or writes to these on-chip registers. The CPU provides the 82557 with the necessary receive and transmit data. The PCI bus interface also provides the means for configuring PCI parameters in the 82557. For more information on PCI, please consult the latest PCI Local Bus Specification (currently Rev. 2.1), available from:

PCI Special Interest Group (SIG)
P.O. Box 14070
Portland, OR 97214
Telephone: (503) 797-4207 (international)
(800) 433-5177 (U.S.)
http://www.pcisig.com

2.1.1.2 Local Memory Interface

The Local Memory Interface provides a glueless connection between the 82557 and external FLASH and/or EEPROM. The FLASH interface, which could also be used to connect to any standard 8-bit EPROM, provides up to 1 Mbyte of addressing to the FLASH. It utilizes a multiplexed address scheme that works in conjunction with a LS373 or compatible latch to demultiplex the address. Both read and write accesses are supported. The FLASH may be used for remote boot functions and network statistics/diagnostics functions. The FLASH is mapped into host system memory (anywhere within the 32-bit memory space) for software accesses. It is also mapped into an available expansion ROM location during boot time of the system. The EEPROM interface is used to store configuration data for the 82557 (i.e. Node Address, board manufacturing ID, etc.).

2.1.2 82557 SERIAL INTERFACE

The 82557 Serial Interface consists of the MII Interface and the Serial (ENDEC) interface. The following table summarizes the serial signals and pins.

Signal Grouping	Signal Name	Corresponding Signal Pin Number
MII Interface		
	Input Clocks (RXCLK, TXCLK)	151, 8
	Receive Data (RXD0-3)	150, 149, 148, 147
	Receive Info. (RXDV, RXER)	153, 152
	Transmit Data (TXD0-3)	7, 6, 3, 2
	Transmit Info. (TXEN)	158
	Link (CRS, COL)	155, 154
	Management (MDIO, MDC)	156, 157
Serial-Side (ENDEC) Interface		
	Input Clocks (RXCLK, TXCLK)	151, 8
	Receive Data (RXD0)	150
	Transmit Data (TXD0)	7
	Transmit Info. (RTS)	158
	Link (CRS, COL)	155, 154
Other		
	(FDX#, FULHAL, RSTOUT, LPBCK)	143, 6, 146, 145

2.1.2.1 MII Interface

The 82557 MII Interface provides the functional interface to any MII compatible PHY. The data path consists of a separate nibble-wide stream for both transmit and receive activities. Data transfers are clocked by the 25 MHz transmit and receive clocks in the 100 Mbps operation, or by 2.5 MHz clocks in the 10 Mbps operation. These clock inputs are driven by the PHY.

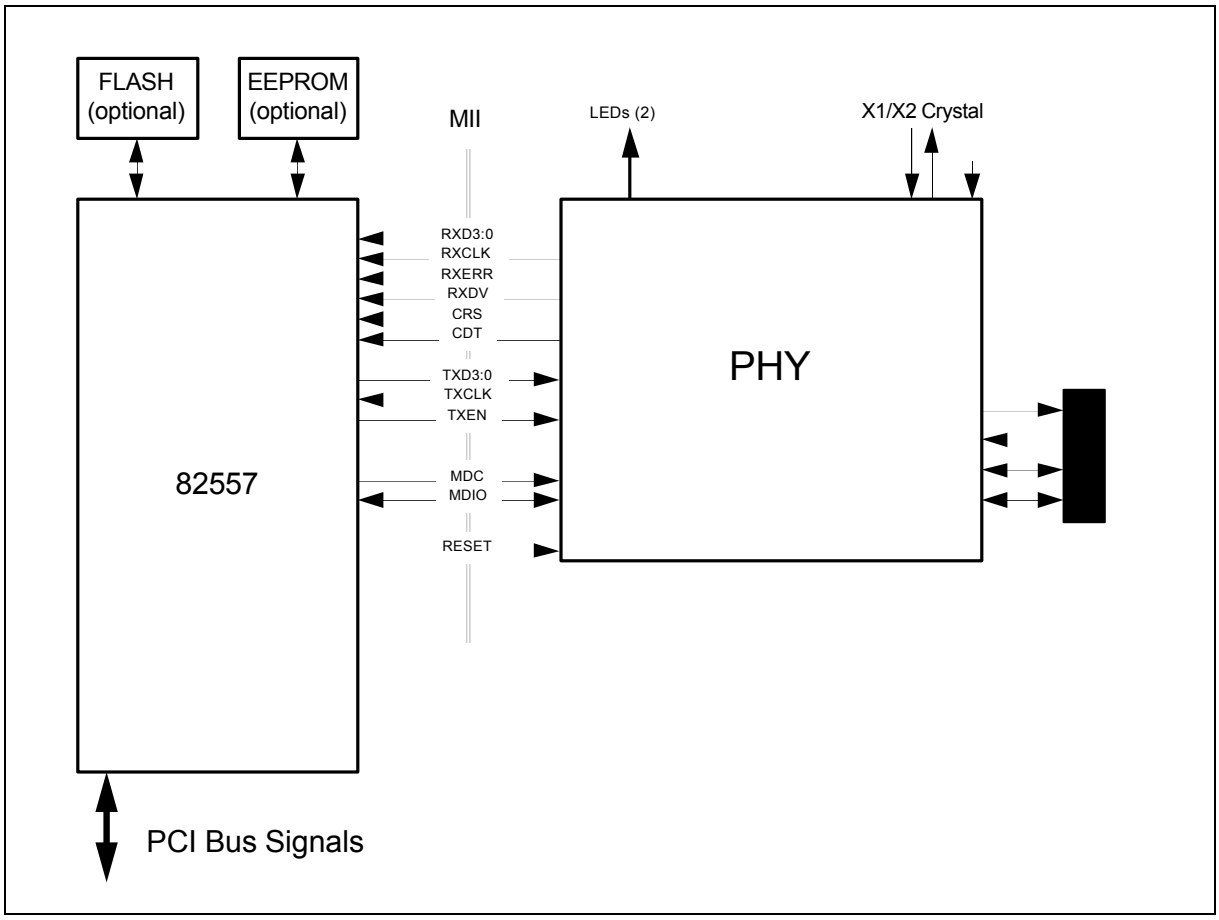
2.1.2.2 Serial Side (ENDEC) Interface

The 82557 Serial-Side interface provides the functional interface to any 10 Mbps (ENDEC) compatible PHY (such as the Intel 82503). The 10 Mbps serial side interface is bit wide.

Transmission is performed on the TXD0 pin and reception on RXD0. Serial data is clocked on the rising edge of the clock (TXCLK for transmission, RXCLK for reception). These clocks operate at the PHY and are both driven by the PHY.

3. THE 82557 AS A LAN SOLUTION

The 82557 provides a complete 10BASE-T or 100BASE-T LAN solution, with the exception of the PHY and magnetics. The following diagram shows a typical design.



3.1 Physical Connections

82557: The 82557 is a 10/100 Mbps PCI LAN controller that consists of a FIFO unit, a Parallel unit, and a Serial unit. It incorporates high-performance and 4-channel DMA Bus Mastering architecture. The 82557 performs the media access control (MAC) functions.

PHY: Physical Layer device interfacing the 82557 and magnetics required for 10BASE-T and/or 100BASE-T operation. The PHY implements physical coding sublayer (PCS) and physical medium attachment (PMA) functions.

Crystal: The crystal provides the clock reference source for the PHY.

EEPROM: The EEPROM contains configuration information for the 82557 as well as the node address (Node ID).

FLASH: The FLASH contains remote boot code, network statistics, diagnostics information. (Note FLASH is optional.)

Magnetics: Magnetics are used to connect to the medium. It provides common mode rejection and wave shape filtering.

3.2 Layout Guidelines

3.2.1 Overview

The LAN designer should follow standard practices for laying out high frequency printed circuit boards (PCB). The designer should take great care in minimizing the effects of cross-talk and propagation delays between the various sections of the board where critical signals are concerned.

All power and ground supply traces should be etched as short and thick as possible. This will help to eliminate the high-frequency crosstalk and noise inherent in high frequency PCB applications. In addition, logic and chassis ground should be connected together as a single plane.

All Vcc pins should be connected to the same power supply and all Vss pins to the same ground plane. All power and ground pins should follow the shortest path to their respective sources. Signal paths to ground in particular should be routed as closely as possible to their source pins in order to avoid ground loops and noise.

All trace bends should be less than 45 degrees in angle.

The following table shows the 82557 power and ground connections.

Signal Grouping	Signal Name	Corresponding Signal Pin Number
Power +5V, ± 5%	Vcc	4, 9, 12, 16, 21, 28, 32, 37, 42, 45, 51, 57, 63, 69, 75, 79, 83, 88, 92, 97, 100, 106, 110, 113, 117,122, 126, 132, 137, 159
Ground	Vss	5, 10, 11, 17, 22, 29, 33, 38, 41, 46, 52, 58, 64, 70, 76, 80, 84, 87, 91, 95, 99, 105, 111, 112, 116, 121, 125, 131, 136, 160

3.2.2 82557 LAN Controller

Since the 82557 is a robust digital integrated circuit, little consideration can be given for its layout. For decoupling, eight 0.1uF capacitors should be placed about the chip at regular intervals to minimize noise. This should be sufficient for proper operation.

3.2.3 Crystal

All physical layer components introduced in this reference design section use crystals to generate clocking signals. Any crystals used should be placed adjacently to the physical layer component and all traces proceeding from it should be as short as possible. The traces should

also be as close in length as possible to reduce the effect of signal propagation delays inherent in high-frequency circuits.

3.2.4 Analog Differential Signals

Each pair of differential signals connected to the analog circuitry (i.e., physical layer analog pins, magnetics pins, and analog connectors) should be etched in parallel about the board wherever possible. These traces must also be as short as possible while being identical in length in order to reduce signal propagation delays and noise within the analog circuitry.

As a general rule, trace widths for these signals should be from one to three times the distance between the PCB layers to eliminate excessive trace inductance which may cause signal noise.

3.2.5 Media Independent Interface (MII)

Since the data lines transmit four bits at a time in parallel, it is necessary to ensure that the traces within each of the data line groups are close together and similar in length and characteristics. This will help to minimize the effects of signal propagation delay and noise.

3.2.6 PCI Bus

As with any high frequency digital device, the traces making up the PCI bus should be relatively similar in length and characteristics. Also, a variety of decoupling capacitors should be used to minimize the effects of noise. It is recommended that at least two 6.8 uF and six 0.1uF capacitors be used to decouple the PCI bus. For any further considerations regarding the PCI bus connections and layout guidelines, please consult the PCI Local Bus Specification.

4. 82557 SCHEMATIC REFERENCE DESIGNS

The following reference designs illustrate design examples using the 82557. For additional information on any non-Intel components (i.e., PHY, magnetics, etc.) please contact the respective vendor of the component.

4.1 100BASE-T4 Designs

4.1.1 Intel 82557 - Seeq 80C240 Design

4.1.1.1 Components

The 80C240 uses a 25 Mhz crystal to generate its internal clock.

An external magnetics component is used by the 80C240 to interface with the LAN. This reference design includes the Pulse Engineering PE69001. Other components may be adequate for this portion of the adapter board, please contact Seeq for more information regarding this. For a description of the PE69001 component, please refer to Pulse Engineering Inc.

Four LED's may be connected to the 80C240 to indicate various operations. The pins driving these LED's are user programmable, but have default values as follows: (1) Link Pulse Detect Output. This LED goes active when a valid link is detected on the LAN. (2) Activity. This LED goes active when a transmit or receive packet has occurred. (3) Full Duplex. This LED is active

when the 80C240 is running in full duplex mode. (4) Speed. This LED indicates the speed of the LAN. It is active during 100 Mbps operation.

Magnetics Vendor/Part Number	Address/Phone
Pulse Engineering Tortuga	1220 World Trade Dr. San Diego, CA 92128 619-684-8100

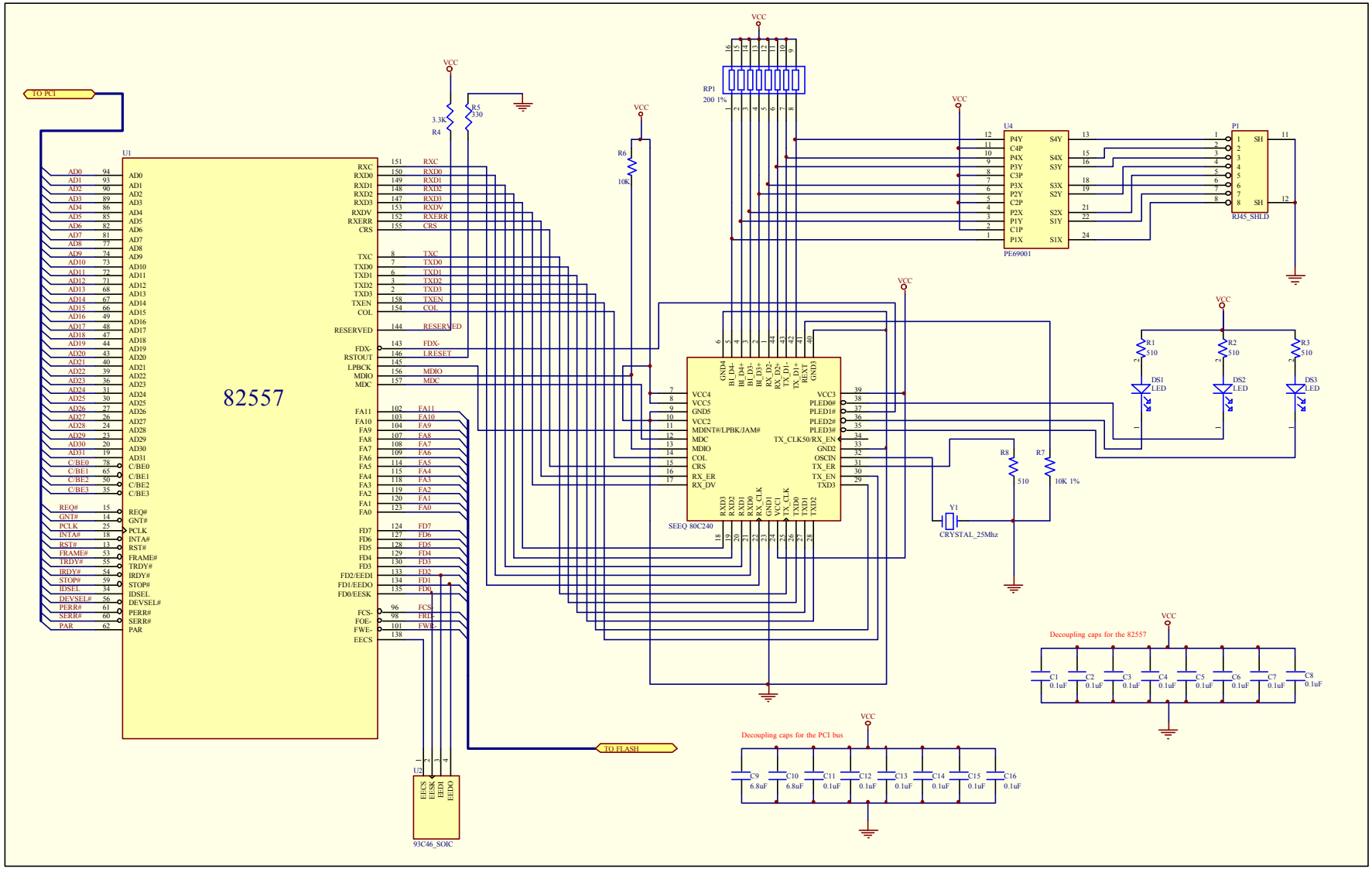


Figure 1. Sample 82557 to Seeq 80C240 Design

4.2 100BASE-TX Design

4.2.1 Intel 82557 - National DP838040 Design

4.2.1.1 Components

The DP83840 uses a 20 Mhz crystal and a 25 Mhz oscillator to generate its internal clocks. For more information regarding the clocking circuitry of the DP83840, contact National Semiconductor.

The DP83840 must be connected to an external physical medium dependent transceiver and magnetics component in order to operate properly. The recommended transceiver is the National DP83223 and the recommended magnetics component is the Pulse Engineering 68515. For a description of these components, contact the vendor listed in the table below.

The DP83840 is able to support five LED's to indicate status to the user or drive an additional component which are defined as follows: (1) Transmit. This LED is active when there is transmit activity and is wire-ored in this design with (2) Receive which is active when there is receive activity on the LAN. (3) Link. This LED is on when there is a valid link to LAN. (4) Full Duplex. This LED indicates full-duplex activity and is used to signal the controller in this application. (5) Collision. This LED indicates a collision condition on the LAN.

Also included in this schematic is a support circuit for the DP83840. This network, consisting of 4 transistors and various resistors and capacitors, is used by the DP83840 to switch between 10 and 100 Mbps operation. For more information regarding this design, contact National Semiconductor.

Magnetics Vendor	Address/Phone
National	2900 Semiconductor Drive P. O. Box 58090 Santa Clara, CA 95052-8089 1-800-272-9959
Valor	9715 Business Park Ave. San Diego, CA 92131 1-800-31-VALOR
Pulse Engineering	1220 World Trade Dr. San Diego, CA 92128 619-684-8100
FEE Fil-Mag USA	9445 Farnham San Diego, CA 92123 619-569-6577

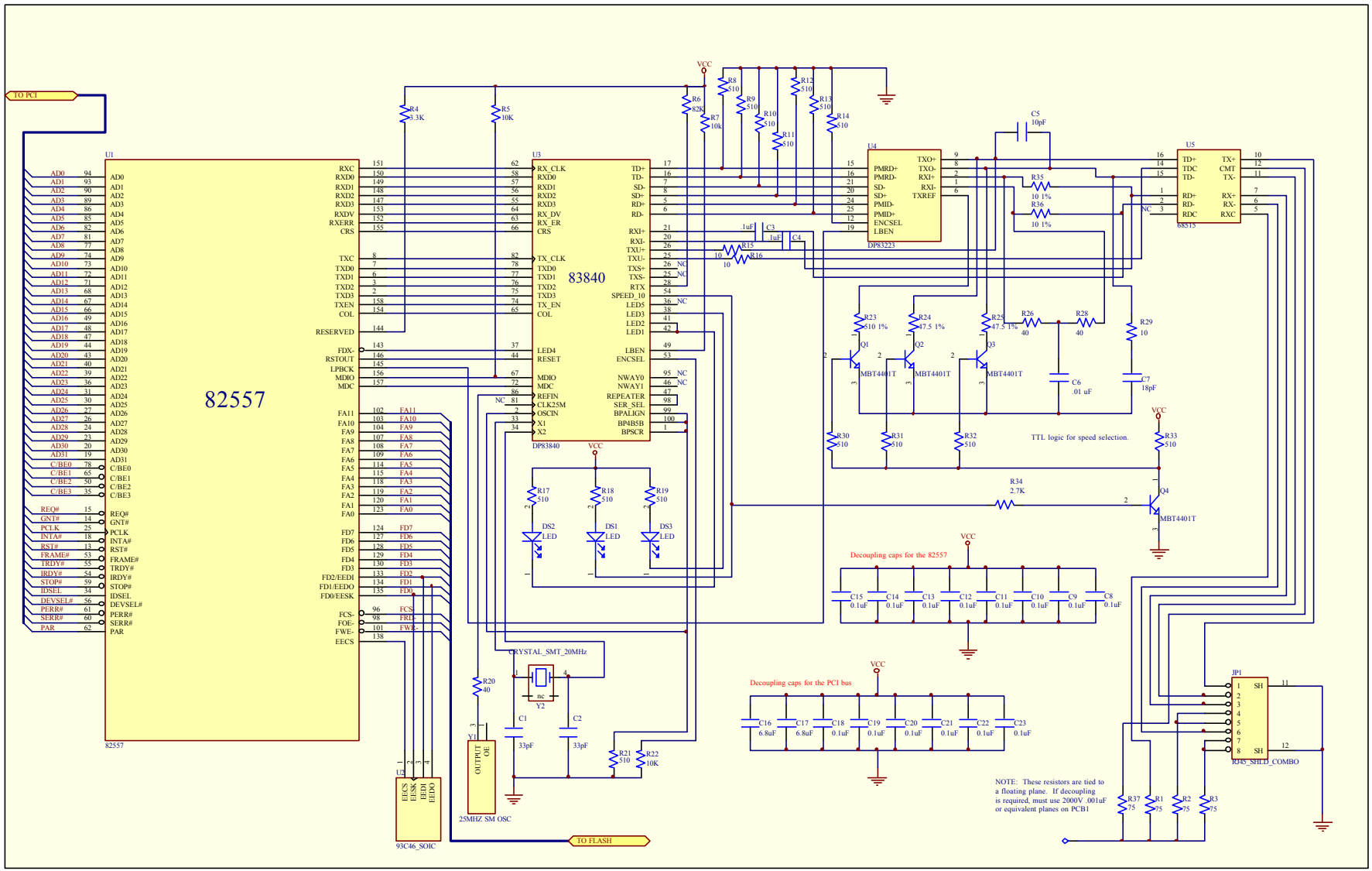


Figure 2. Sample 82557 to National DP838040 Design

4.2.2 Intel 82557 - MII Design

This reference design consists of the 82557 interfaced to the MII connector.

4.2.2.1 Components

A bank of 39 ohm resistors is placed between the MII output pins and the MII connector to take account of the characteristic impedance of the cable (defined in the MII specification to be 68 ohms ± 15%) and the output source impedance of the 82557.

A physical layer transceiver device is used to interface the 82557/MII design to the wire. The following vendors provide various transceiver devices (100BASE-TX, 100BASE-T4, 100BASE-FX):

Transceiver Vendor	Address
Allied Telesyn	950 Kifer Road Sunnyvale, CA 94086
LANCAST	10 Northern Blvd. Unit 5 Amherst, NH 03031 (800) 9-LANCAST
Digi International (MiLAN Technology)	1299 Orleans Sunnyvale, CA 94089 1-800-466-4526

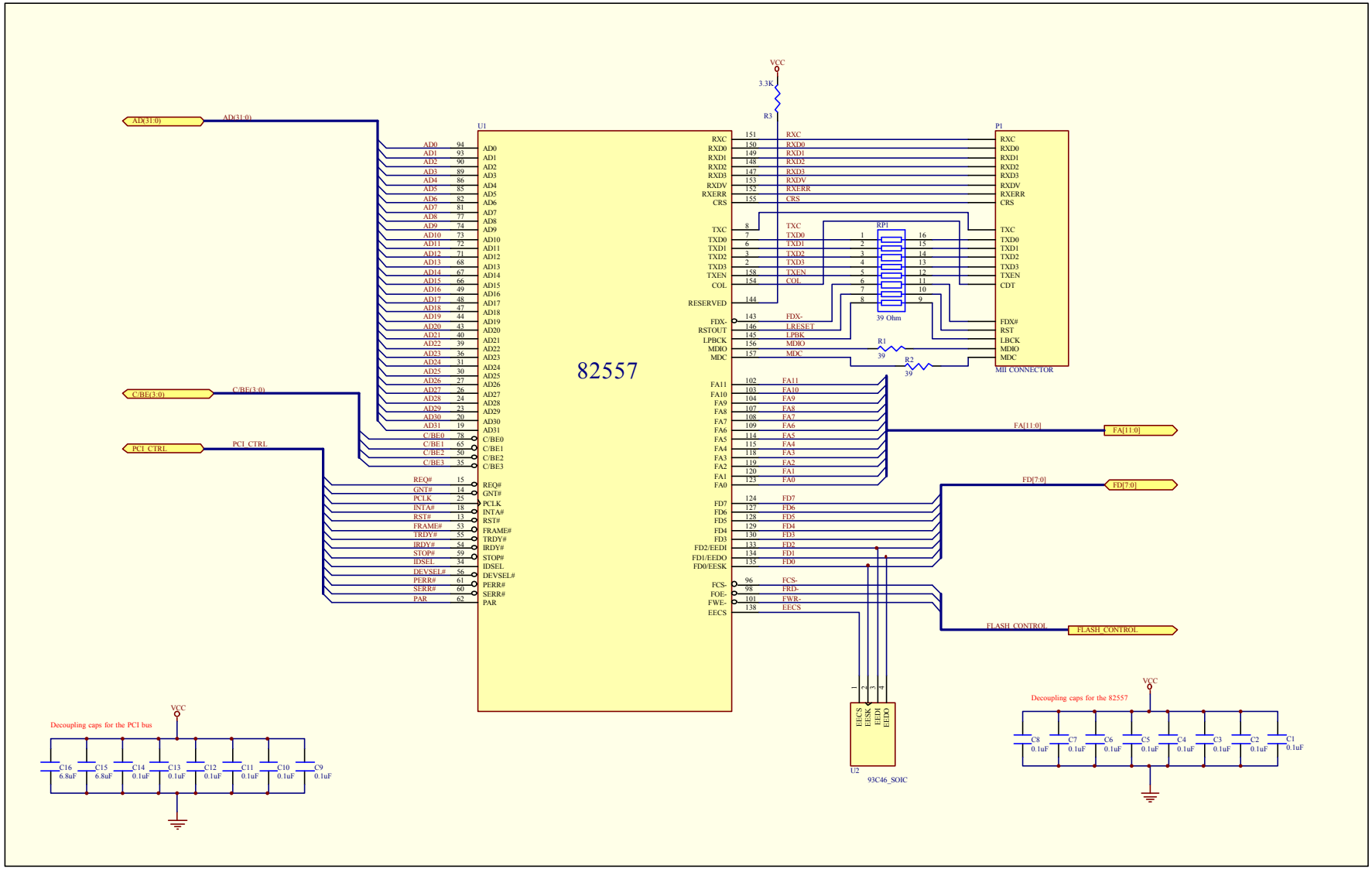


Figure 3. Sample 82557 to MII Design

5. 82557 BILL OF MATERIALS

This section provides a bill of materials for each reference design covered in this application note.

5.1 BILL OF MATERIALS FOR 82557 - Seeq 80C240 REFERENCE DESIGN

PART	DESIGNATOR
CAP 6.8 uF TANT, 25v *	C9 C10
CAP 0.1uF X7R 20% *	C1 C2 C3 C4 C5 C6 C7 C8 C11 C12 C13 C14 C15 C16
RES 3.3K 5% 1/10W	R4
RES 10R 5% 1/10W	R2 R6
RES 10R 1% 1/10W	R7
RES 330R 5% 1/10W	R5
RES 392R 5% 1/10W	R1 R3
RES 510R 5% 1/10W	R8 R9 R10 R11
RES 8-PACK 200R 1% 1/10W	RP1
.01% 25MHZ Crystal	Y1
Dialight 595-2301 LED	DS1 DS2 DS3
RJ45	P1
Intel S82557 Fast Ethernet Controller	U1
SEEQ 80C240 Physical Layer	U3
National Semiconductor NM93C46M8 Serial EEPROM[1]	U2
Pulse Engineering PE69001 Transformer	U4

* These capacitors are used for decoupling only.

1. The following vendors also supply this part:

VENDOR	PART NO.
National Semiconductor	NM93C46M8-TR
Samsung Corning Co.	KM93C46GD-T
National Semiconductor	NM93C14M8-TR
Samsung Corning Co.	XL93LC46ARF-111

5.2 BILL OF MATERIALS FOR 82557 - NATIONAL DP83840 REFERENCE DESIGN

PART	DESIGNATOR
CAP 0.1uF X7R 20%	C3 C4
CAP 0.01 uF X7R 10%	C6
CAP 10 pF COG 5%	C5
CAP 18 pF COG 5%	C7
CAP 33 pF COG 5%	C1 C2
CAP 0.1uF X7R 20% *	C8 C9 C10 C11 C12 C13 C14 C15 C18 C19 C20 C21 C22 C23
CAP 6.8 uF TANT, 25v *	C16 C17
RES 2.7K 5% 1/10W	R34
RES 3.3K 5% 1/10W	R4
RES 10R 5% 1/10W	R15 R16 R29
RES 10K 5% 1/10W	R2 R5 R7 R22
RES 40R 5% 1/10W	R20 R26 R28
RES 47.5R 1% 1/10W	R24 R25
RES 75R 5% 1/10W	R37 R38 R39 R40
RES 82K 5% 1/10W	R6
RES 10R 1% 1/10W	R35 R36
RES 392R 5% 1/10W	R1 R3
RES 510R 5% 1/10W	R8 R9 R10 R11 R12 R13 R14 R17 R18 R19 R21 R30 R31 R32 R33
RES 510R 1% 1/10W	R23
Toyocom TCO-711JTCR-25MHZ .01% 25MHZ Oscillator[1]	Y1
KDS DX200-20 TR 20Mhz Crystal[2]	Y2
Central Semiconductor CMPT4401 TR Transistor[3]	Q1 Q2 Q3 Q4
Dialight 595-2301 LED	DS1 DS2 DS3
RJ45	P1
Intel S82557 Fast Ethernet Controller	U1
National DP83840 Physical Layer	U3
National Semiconductor NM93C46M8 Serial EEPROM[4]	U2
National DP83223 Twister	U4
Pulse Engineering PE68515 Transformer	U5

* These capacitors are used for decoupling only.

1. The following vendors also supply this part:

VENDOR	PART NO.
Kyocera	AMO-HC1-CSE-25MHZ
Epson America Inc.	SG-615P-25MHZ

2. The following vendors supply this part:

VENDOR	PART NO.
Fox International	FPX200-20 TR
Epson America Inc.	MA506 20.000MG$ TR
Raltron	TT-SMD 20MHZ 20PF TR
Monitor Products Com.	SM-55N1B7E20.000MHZ
M-TRON	SX2050-20MHZ-20PF TR
ECS Inc.	ECS-200-20PF-7-TR

3. The following vendors also supply this part:

VENDOR	PART NO.
National Semiconductor	MMBT4401 TR
Motorola	MMBT4401LT1
Diodes Inc./Liteon	IMBT4401 TR
Rohm Corp.	SST4401$

4. The following vendors also supply this part:

VENDOR	PART NO.
National Semiconductor	NM93C46M8-TR
Samsung Corning Co.	KM93C46GD-T
National Semiconductor	NM93C14M8-TR
Samsung Corning Co.	XL93LC46ARF-111

5.3 BILL OF MATERIALS FOR 82557 - MII REFERENCE DESIGN

PART	DESIGNATOR
CAP 0.1uF X7R 20% *	C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14
CAP 6.8 uF TANT, 25v *	C15 C16
RES 3.3K 5% 1/10W	R6
RES 10K 5% 1/10W	R4
RES 39R 5% 1/10W	R1 R2
RES 392R 5% 1/10W	R3 R5
RES PACK 39R 5% 1/10W	RP1
Intel S82557 Fast Ethernet Controller	U1
National Semiconductor NM93C46M8 Serial EEPROM[1]	U2
AMP Inc. 535512-07 Connector	P1

* These capacitors are used for decoupling only.

1. The following vendors also supply this part:

VENDOR	PART NO.
National Semiconductor	NM93C46M8-TR
Samsung Corning Co.	KM93C46GD-T
National Semiconductor	NM93C14M8-TR
Samsung Corning Co.	XL93LC46ARF-111