SIEMENS

ICs for Communications
ISDN Subscriber Access Controller for U_{pn}-Interface Terminals

SmartLink-P
PSB 2197

User's Manual 02.95

PEB 2197 Revision History: Original Version: 02.95	
Previous Releases:	
Page	Subjects (changes since last revision)

Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

For detailed technical information about **"Processing Guidelines"** and **"Quality Assurance"** for ICs, see our **"Product Overview"**.

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Introduction

The PSB 2197, SmartLink-P, implements the subscriber access functions for a digital terminal to be connected to a two-wire U_{pn}-interface.

The PSB 2197 SmartLink-P is an optimized device for TE-applications, covering the complete layer-1 and basic layer-2 functions for digital terminals.

The PSB 2197 SmartLink-P combines the functions of the U_{pn}-transceiver with reduced loop length (one channel of the OCTAT®-P PEB 2096) and a simple HDLC-controller for signaling data onto one chip.

A pulse width modulator is included to provide an LCD-contrast control or a ring tone signal.

The serial control port of the SmartLink-P is compatible to most serial interfaces of microcontrollers. In addition it provides the microcontroller clock signal as well as an undervoltage detector and reset generation including a watchdog function.

The Terminal Repeater function of the SmartLink-P allows to cascade two telephones which are controlled by one U_{pn}-interface from the line card or to extend the loop length by using an IEC-Q transceiver.

The SmartLink-P can also be used as a simple HDLC-controller which provides the TIC-bus access procedure. In this mode, the U_{pn}-transceiver is inactive.

The PSB 2197 SmartLink-P interfaces to voice/data devices via the IOM®-2 interface and provides an additional bit clock and strobe signal for standard codecs. The upstream B-channel information may be muted or loop back the downstream data.

The PSB 2197 SmartLink-P is a 1-micron CMOS device offered in a P-DSO-28 package. It operates from a single 5-V supply.

Note: U_{pn} in the document refers to a version of the U_{p0}-standard with a reduced loop length.

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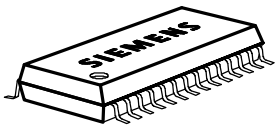
ISDN Subscriber Access Controller for U_{pn}-Interface Terminals (SmartLink-P)

PSB 2197

Preliminary Data

CMOS IC

1 Features



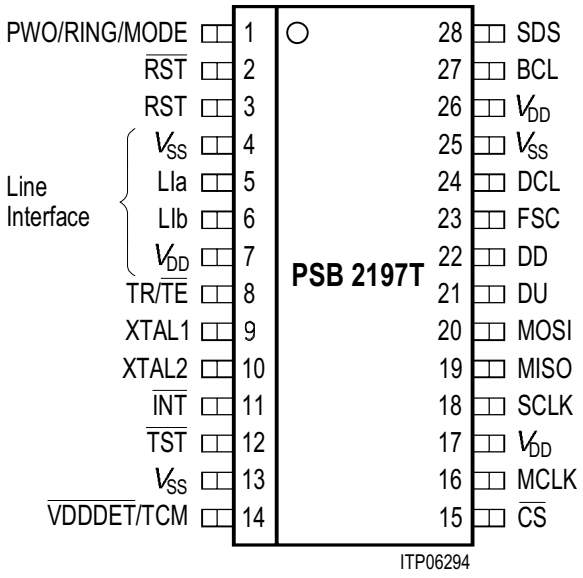
P-DSO-28-1

- Cost/performance-optimized U_{pn}-interface transceiver, compatible to PEB 2096 OCTAT-P and PSB 2195 ISAC®-P or PSB 2196 ISAC®-P TE
- HDLC-controller with 2 × 4 byte FIFO per direction
- IOM®-2 interface for terminal application including bit clock and strobe signal
- Uplink MUTE function
- Selective B-channel loop back
- Serial control port
- Pulse width output LCD-contrast control or ring tone generation
- CPU-clock and reset output
- Watchdog timer
- Test loops
- Advanced CMOS-technology
- Low power consumption: active: 100 mW max.

Type	Ordering Code	Package
PSB 2197T	Q67100-H6462	P-DSO-28-1 (SMD)

Pin Configurations
(top view)

P-DSO-28-1



1.1 Pin Definitions and Functions

Pin No.	TE-Mode		TR-Mode		HDLC-Controller Mode		
P-DSO-28	Symbol	Input (I) Output (O) Open Drain (OD)	Symbol	Input (I) Output (O) Open Drain (OD)	Symbol	Input (I) Output (O) Open Drain (OD)	Function
15	$\overline{CS}$	I	$\overline{CS}$	I	$\overline{CS}$	I	**Chip Select.** A low level indicates a microprocessor access to the SmartLink-P. It masks the $\overline{INT}$-output.
11	$\overline{INT}$	OD	$\overline{INT}$	OD	$\overline{INT}$	OD	**Interrupt Request.** $\overline{INT}$ becomes active if the SmartLink-P requests an interrupt. $\overline{INT}$ is masked by $\overline{CS}$.
16	MCLK	O	0, low	O	0, low	O	**Microprocessor Clock.** Clock output for the microcontroller.
3	RST	O	inv. $\overline{RST}$	O	inv. $\overline{RST}$	O	**Reset.** High active reset output. In TR-mode and HDLC-controller mode, RST outputs the inverse of the $\overline{RST}$-input.
2	$\overline{RST}$	I/O (OD)	$\overline{RST}$	I	$\overline{RST}$	I	**Reset.** Low active reset output and input (TE, open drain), low active reset input in TR-mode.
8	TR/$\overline{TE}$ (V_{SS})	I	TR/$\overline{TE}$ (V_{DD})	I	TR/$\overline{TE}$ (V_{DD})	I	**Terminal Repeater/ TE-Mode Selection.** Selects terminal repeater mode (V_{DD}) or TE-mode (V_{SS}).

Pin Definitions and Functions (cont'd)

Pin No.	TE-Mode		TR-Mode		HDLC-Controller Mode		
P-DSO-28	Symbol	Input (I) Output (O) Open Drain (OD)	Symbol	Input (I) Output (O) Open Drain (OD)	Symbol	Input (I) Output (O) Open Drain (OD)	Function
20	MOSI	I	MOSI	I	MOSI	I	**Master Out Slave In.** Receive data line of the serial control interface. Operates only as slave.
19	MISO	O	MISO	O	MISO	O	**Master In Slave Out.** Transmit data line of the serial control interface. Operates only as slave. MISO is tristate while $\overline{CS}$ is high.
18	SCLK	I	SCLK	I	SCLK	I	**Serial Clock.** Clock signal of the serial control interface.
22 21	DD DU	I/O (OD) I/O (OD)	DD DU	I/O (OD) I/O (OD)	DD DU	I/O (OD) I/O (OD)	**Data Downstream.** **Data Upstream.** Transfer the data of the IOM-2 interface. External pull-up resistors in the range of 4.7 kΩ to 820 Ω are required.

Pin Definitions and Functions (cont'd)

Pin No.	TE-Mode		TR-Mode		HDLC-Controller Mode		
P-DSO-28	Symbol	Input (I) Output (O) Open Drain (OD)	Symbol	Input (I) Output (O) Open Drain (OD)	Symbol	Input (I) Output (O) Open Drain (OD)	Function
9	XTAL1	I	XTAL1	I	XTAL1	I	**Crystal 1.** Connection for a crystal or used as external clock input. For HDLC-controller mode XTAL1 requires a clock signal of at least 80 clock periods after reset.
10	XTAL2	O	XTAL2	O		O	**Crystal 2.** Connection for a crystal. Not connected if an external clock is supplied on XTAL1. (TE & TR-mode)
24	DCL	O	DCL	I	DCL	I	**Data Clock**. IOM-interface clock signal. Clock frequency is twice the IOM-data rate. TE: clock output IOM-2: 1536 kHz TR, HDLC: clock input IOM-2: 1536 kHz
23	FSC	O	FSC	I	FSC	I	**Frame Sync.** **TE:** Frame synchronization output. High during IOM-channel 0 on the IOM-2 interface. **TR, HDLC:** Input synchronization signal IOM-2 mode.

Pin Definitions and Functions (cont'd)

Pin No.	TE-Mode		TR-Mode		HDLC-Controller Mode		
P-DSO-28	Symbol	Input (I) Output (O) Open Drain (OD)	Symbol	Input (I) Output (O) Open Drain (OD)	Symbol	Input (I) Output (O) Open Drain (OD)	Function
5 6	LIa LIb	I/O I/O	LIa LIb	I/O I/O	LIa LIb	I/O I/O	**Line Interface a.** **Line Interface b.** U_{pn}-transceiver signals. In HDCL-controller mode both pins must be connected via a 10 kΩ resistor.
27	BCL	O	0, low	O	BCL	O	**Bit Clock.** IOM-bit clock signal (768 kHz) in TE- and HDLC-controller mode if programmed by SDS-bits. In TR-mode, the default value of CTRL4 fixes BCL to '0'.
28	SDS	O	0, low	O	SDS	O	**Serial Data Strobe.** Strobe signal to indicate 64 kbit/s time-slot in TE- and HDLC-mode. In TR-mode, the default value of CTRL4 fixes SDS to '0'.
1	PWO/ RING	O	HDLC/ $\overline{TR}$	I	HDLC/ $\overline{TR}$	I	**Pulse Width Output/Ring/Mode.** Provides the output of the pulse width modulator or ring tone generator. Selects between HDLC-(1) and TR-(0) mode if TR/$\overline{TE}$ = 1.

Pin Definitions and Functions (cont'd)

Pin No.	TE-Mode		TR-Mode		HDLC-Controller Mode		
P-DSO-28	Symbol	Input (I) Output (O) Open Drain (OD)	Symbol	Input (I) Output (O) Open Drain (OD)	Symbol	Input (I) Output (O) Open Drain (OD)	Function
14	$\overline{\text{VDDDET}}$	I	TCM	I	$\overline{\text{VDDDET}}$	I	**$\overline{\text{VDDDET}}$/T-Channel Mode.** In TE- and HDLC-mode, this pin selects if the V_{DD} detection is active ('0') and reset pulses are generated or whether it is deactivated ('1') and an external reset has to apply on pin $\overline{\text{RST}}$. In TR-mode, TCM is used to select the T-channel source (S/G or '1').
12	$\overline{\text{TST}}$	I	$\overline{\text{TST}}$	I	$\overline{\text{TST}}$	I	**Test Pin.** This input is used to select the test mode register via the serial interface. See test mode description. For normal operation, this pin must be tied to high (V_{DD}).
7, 17, 26	V_{DD}		V_{DD}		V_{DD}		**Power Supply** (+ 5 V ± 5 % (U_{pn}-specification), ± 10 % operational).
4, 13, 25	V_{SS}		V_{SS}		V_{SS}		**Ground.**

Please note that pin 4 and pin 7 are the supply pins for the analog drivers LIa/b. They are disconnected internally from the other supply pins except for the ESD-protection circuitry.

To overcome ESD-problems it is necessary to put series resistors in the low voltage output drivers. The resistor value is in range 40 to 50 Ω. The following output drivers will have these resistors: $\overline{\text{INT}}$, MCLK, RST, $\overline{\text{RST}}$, MISO, BCL, SDS, PWO/Ring/MODE. The resistor doesn't affect the high voltage output driver.

The following output drivers will not have the resistors: DD, DU, XTAL2, LIa, LIb.

1.2 Logic Symbol

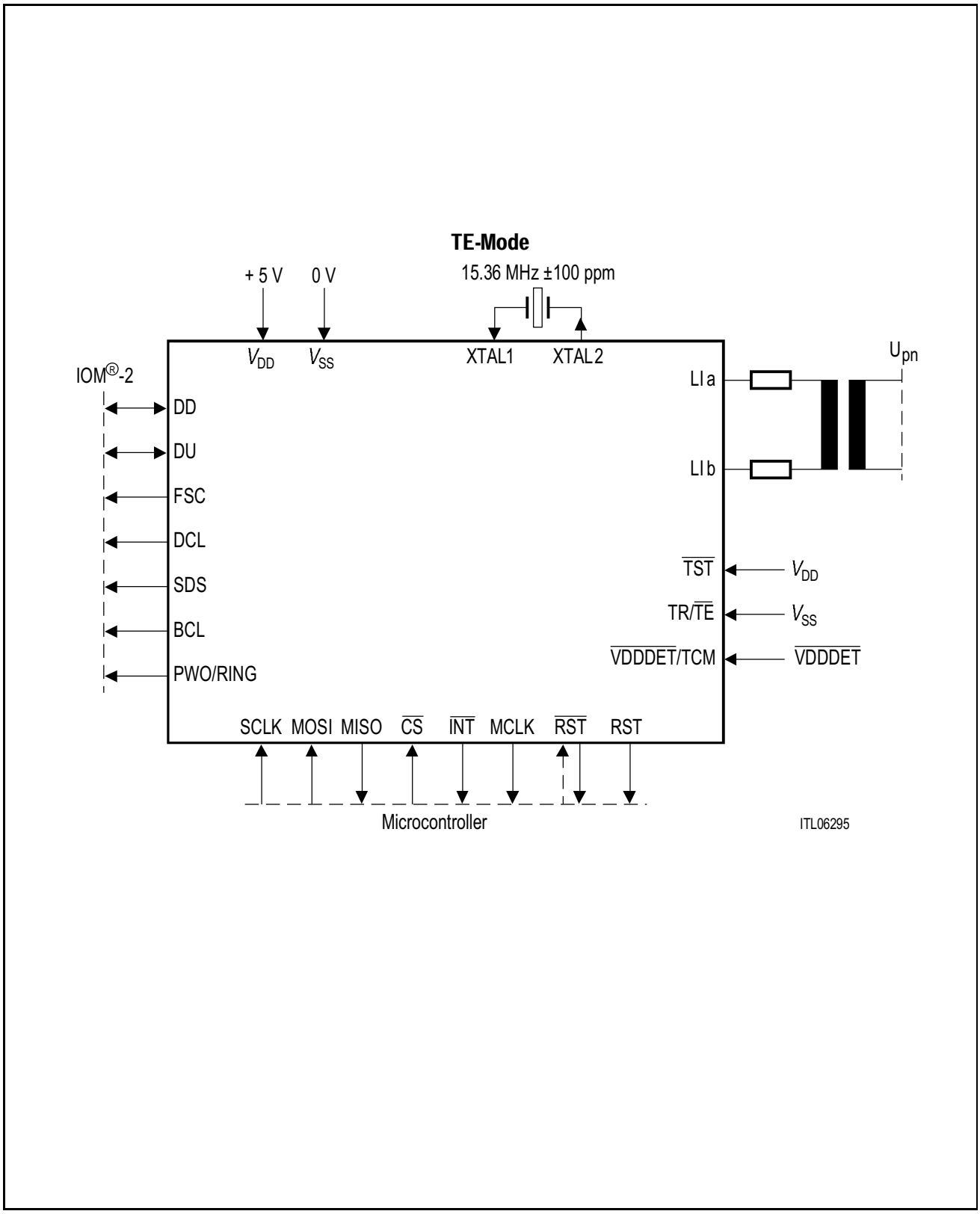


Figure 1
Logic Symbol of the SmartLink-P TE-Mode

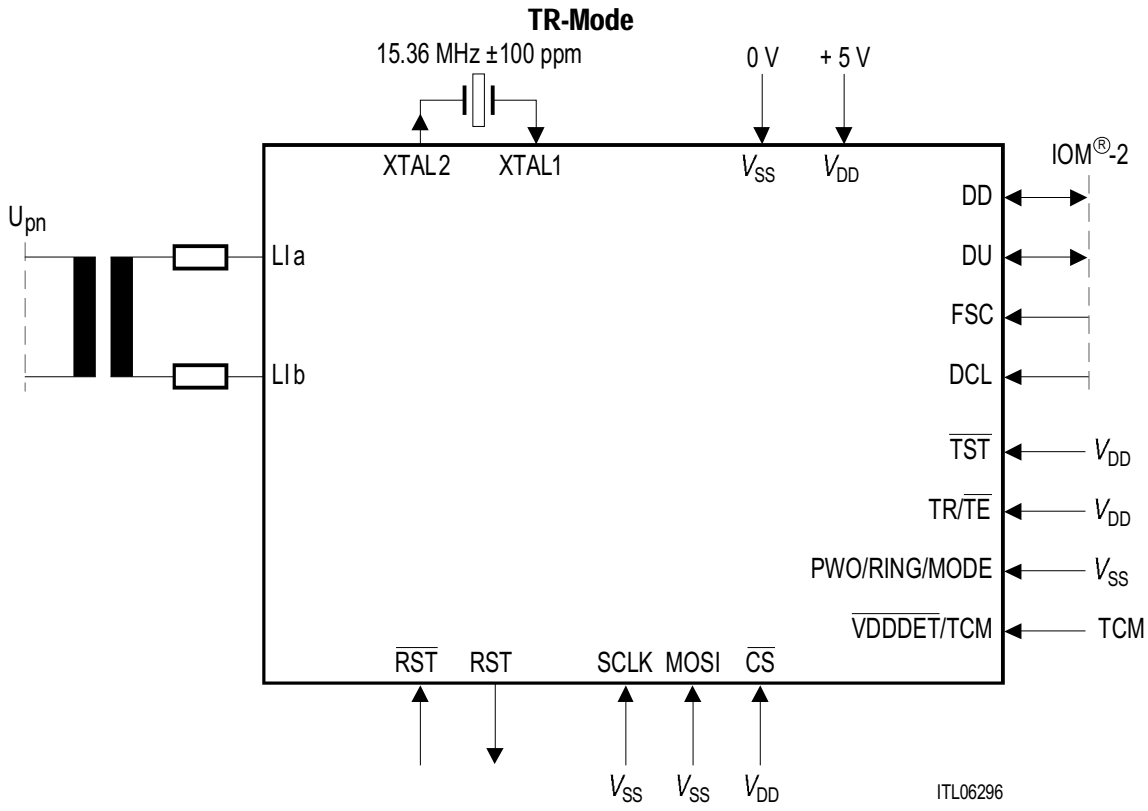


Figure 2
Logic Symbol of the SmartLink-P TR-Mode

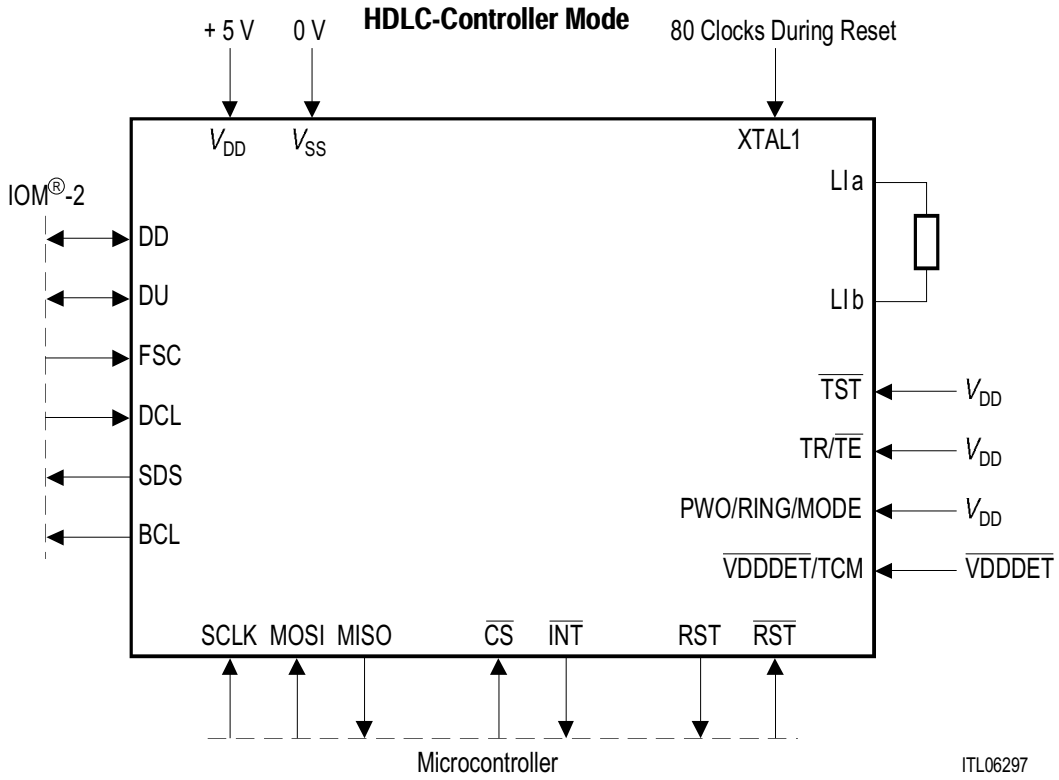


Figure 3
Logic Symbol of the SmartLink-P HDLC-Controller Mode

1.3 Functional Block Diagram

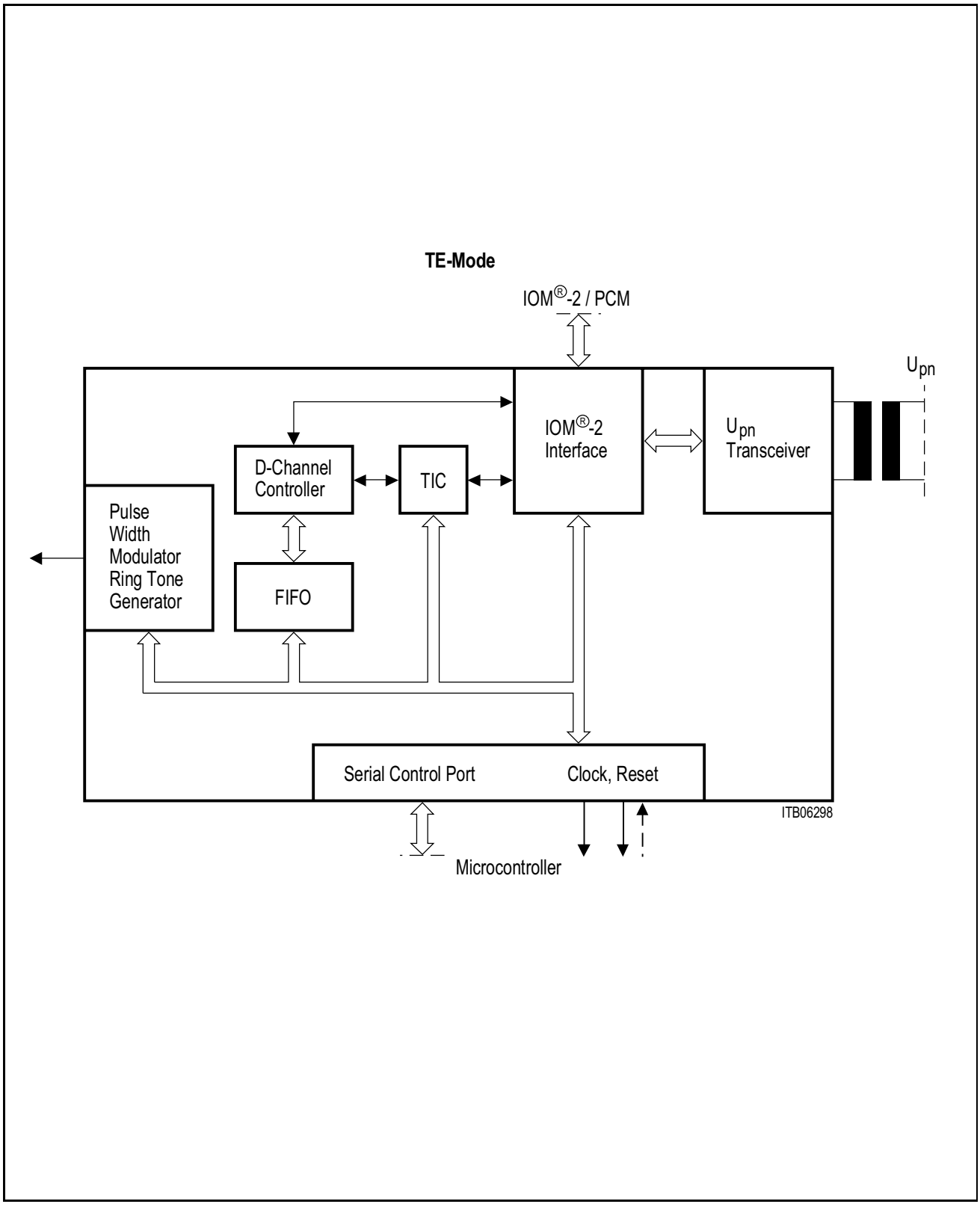


Figure 4
Block Diagram of the SmartLink-P TE-Mode

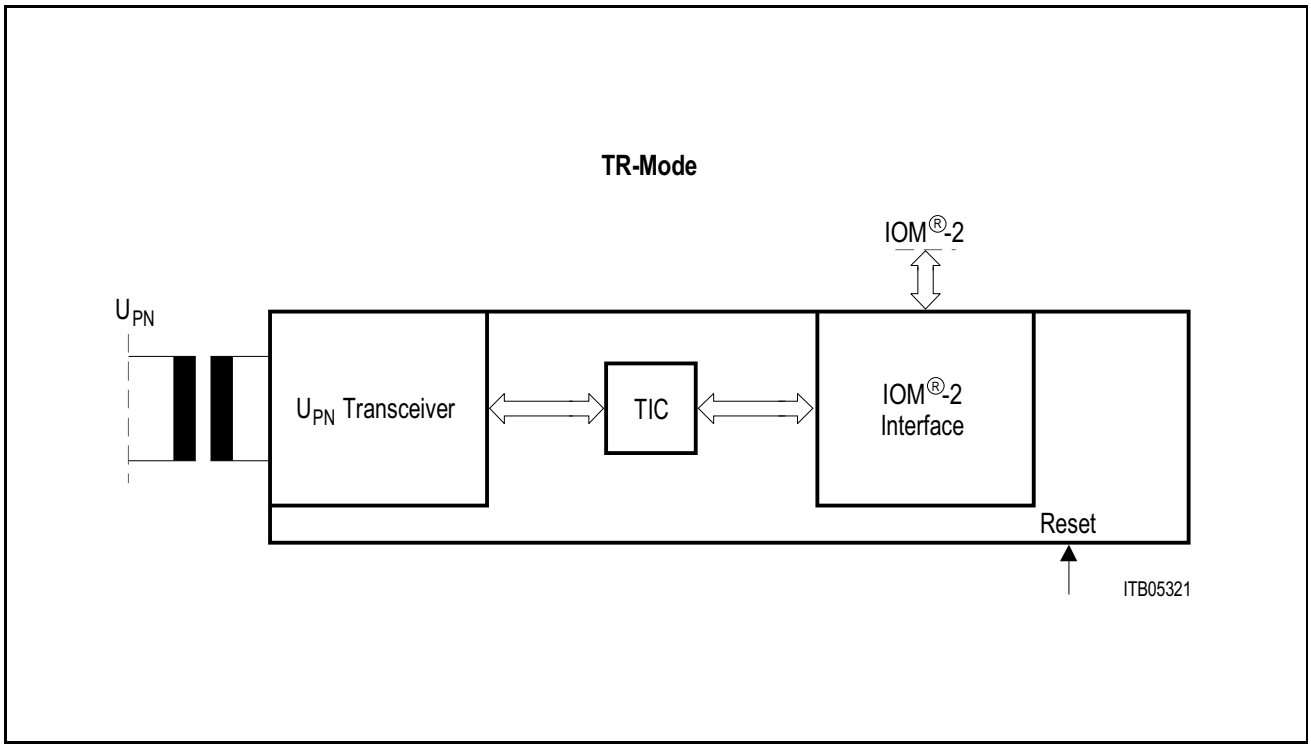


Figure 5
Block Diagram of the SmartLink-P TR-Mode

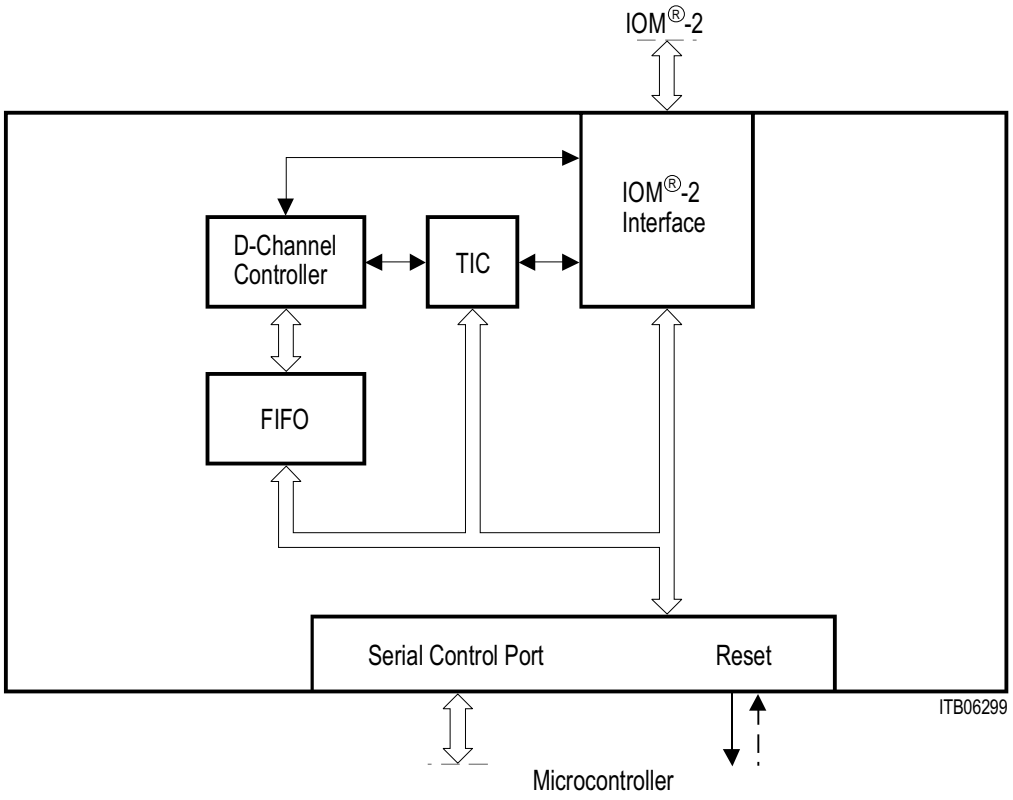


Figure 6
Block Diagram of the SmartLink-P HDLC-Controller Mode

1.4 System Integration

1.4.1 Low Cost Digital Telephone Using the SmartLink-P

A low cost digital telephone behind a PBX consists of the SmartLink-P, a standard codec and a microcontroller with on-chip ROM. This architecture is shown in **figure 7**. The SmartLink-P performs the conversion between the U_{pn}-interface and the IOM-2 interface of the B-channel and D-channel information. The D-channel signaling information is processed by an HDLC-controller inside the SmartLink-P which provides 2×4 byte FIFOs in each direction. The serial strobe signal controls the time-slot which is used by the codec.

A frequency signal generated by the SmartLink-P can be used for ring tone generation. The C510 family of microcontrollers are versions of the standard C501 core enhanced by the synchronous serial interface (SSI).

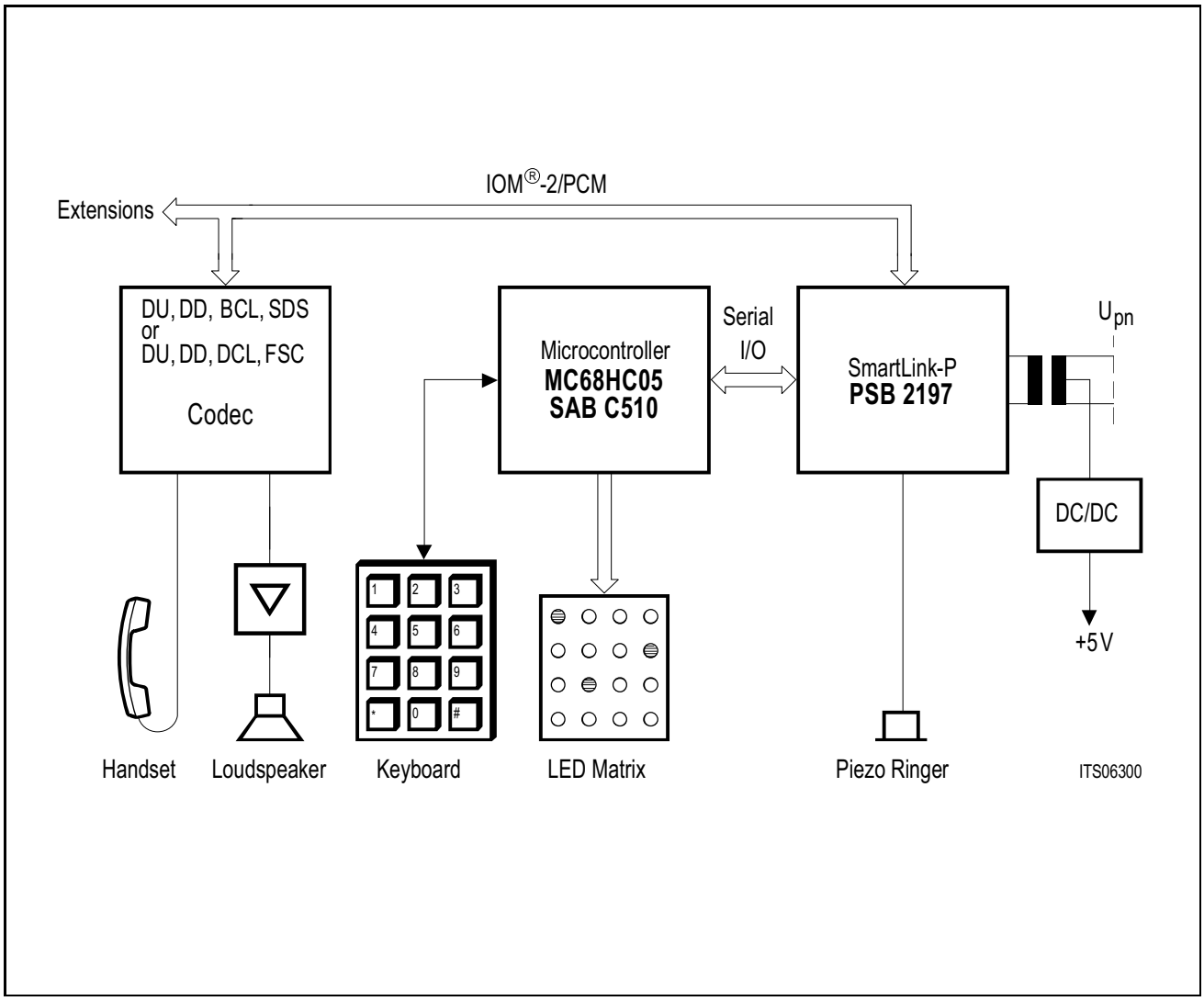


Figure 7
Low Cost Digital Telephone Using the SmartLink-P

1.4.2 Low Cost Digital Feature Phone Using the SmartLink-P

A low cost digital feature phone behind a PBX consists of the SmartLink-P, a feature codec like the ARCOFI®-SP PSB 2163 and a microcontroller with on-chip ROM. This architecture is shown in **figure 8**. The SmartLink-P performs the conversion between the U_{pn}-interface and the IOM-2 interface of the B-channel and D-channel information. The D-channel signaling information is processed by an HDLC-controller inside the SmartLink-P which provides 2×4 byte FIFOs in each direction. The parallel microcontroller interface is designed in a way to share the control lines with an LCD-display controller reducing the required number of I/O-lines. A pulse width modulated signal can be used to control the contrast of an LCD-display.

The C510 family of microcontrollers are versions of the standard C501 core enhanced by the synchronous serial interface (SSI).

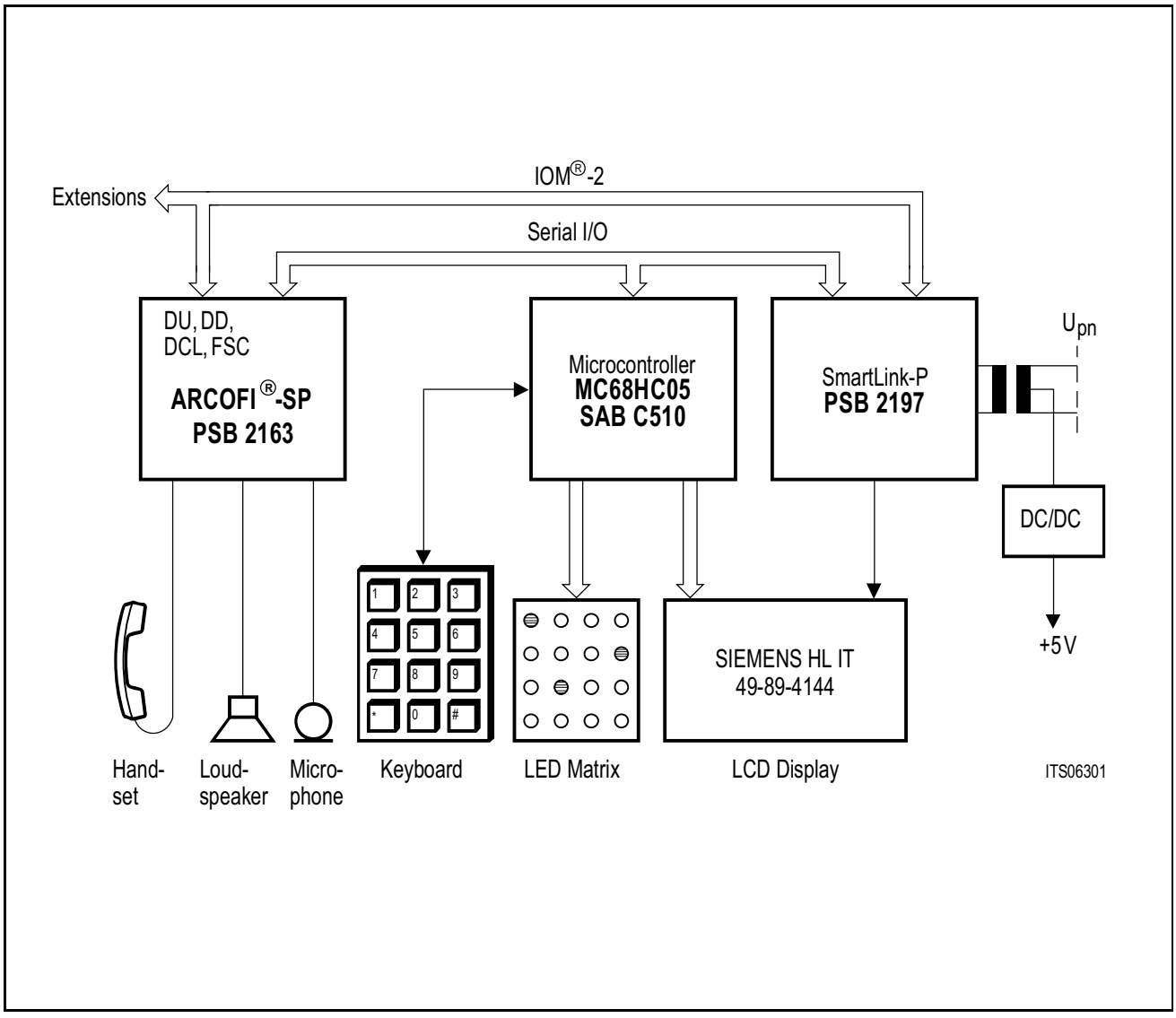


Figure 8
Low Cost Digital Feature Phone Using the SmartLink-P

1.4.3 U_{pn}-Terminal Repeater

The SmartLink-P is designed to operate as a U_{pn}-terminal repeater (**figure 9**). It provides a mechanism to control further U_{pn}-terminals by using the T-channel of the U_{pn}-interface and the TIC-bus on the IOM-2 interface.

The terminal repeater function allows to cascade two U_{pn}-telephones up to a loop length of 100 m.

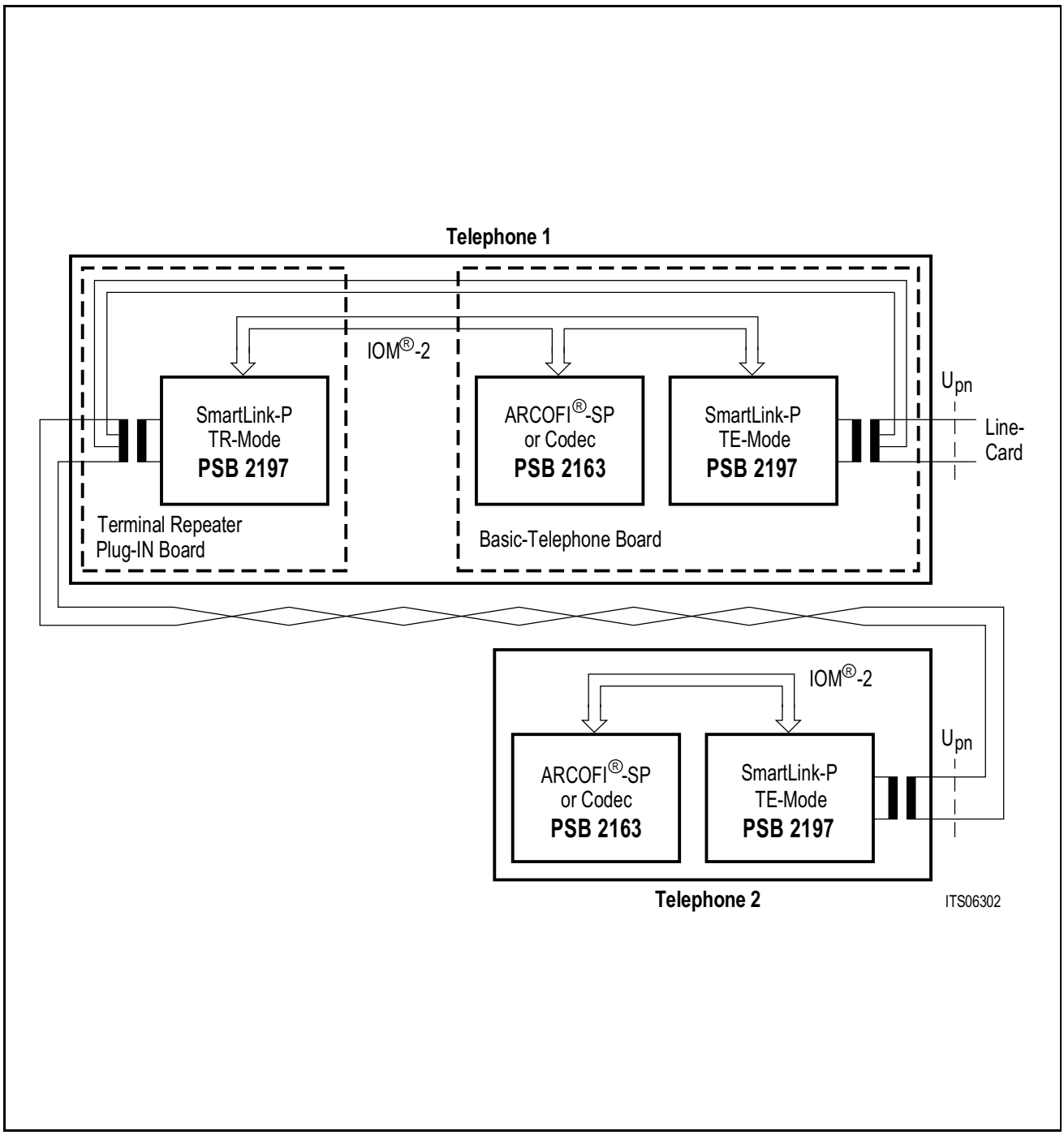


Figure 9
U_{pn}-Terminal Repeater

1.4.4 Network Termination Module

The combination of the PEB 2091 (IEC-Q) and PSB 2197 (SmartLink-P) allows the extension of the loop length between the line card and U_{pn}-terminals up to 8 km. The SmartLink-P provides the regular U_{pn}-interface to connect standard U_{pn}-terminals to it.

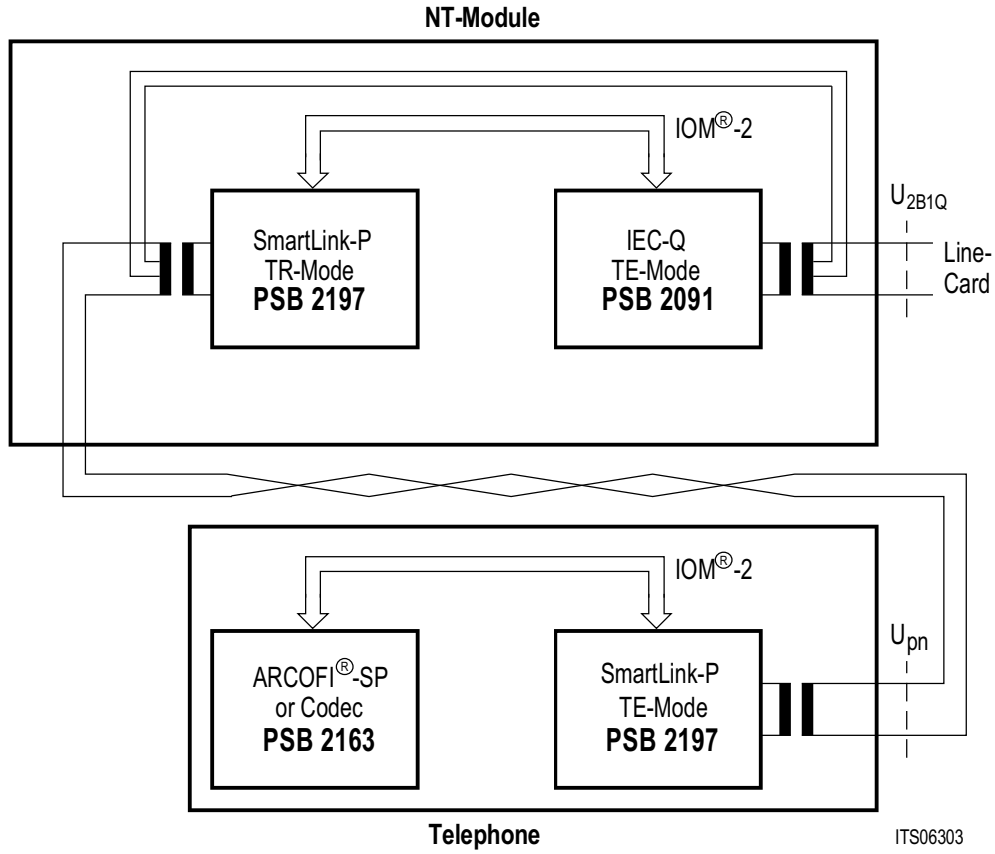


Figure 10
Network Termination Using the SmartLink-P

1.4.5 S/T-Interface Option

A telephone based on the SmartLink-P may be extended by an S/T-interface option to connect standard S/T-interface terminals like ISDN PC cards or videophones to it (**figure 11**). This option uses a PSB 20810 (mask version of the SBCX, PEB 2081) for the S/T-interface. The D-channel arbitration between the D-channel controller of the SmartLink-P and the upstream D-channel data of the S/T-interface is done by the TIC-bus of the IOM-2 interface.

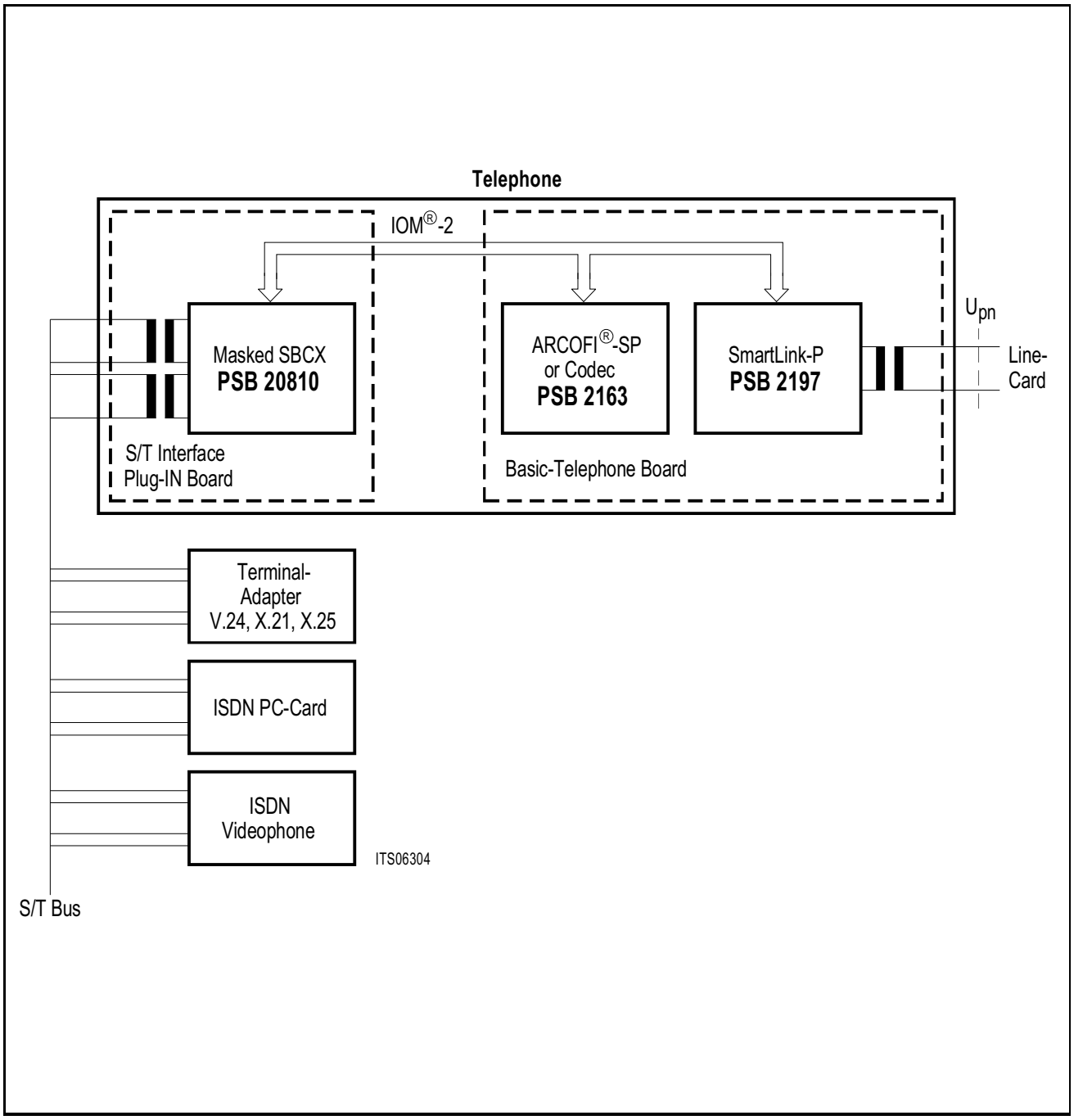


Figure 11
U_{pn}-Telephone with S/T-Interface Option

1.4.6 HDLC-Controller on IOM®-2 Extensions

The SmartLink-P can be used as a HDLC-controller to access the D-channel via the TIC-bus procedure. In this mode, the U_{pn}-interface is not active.

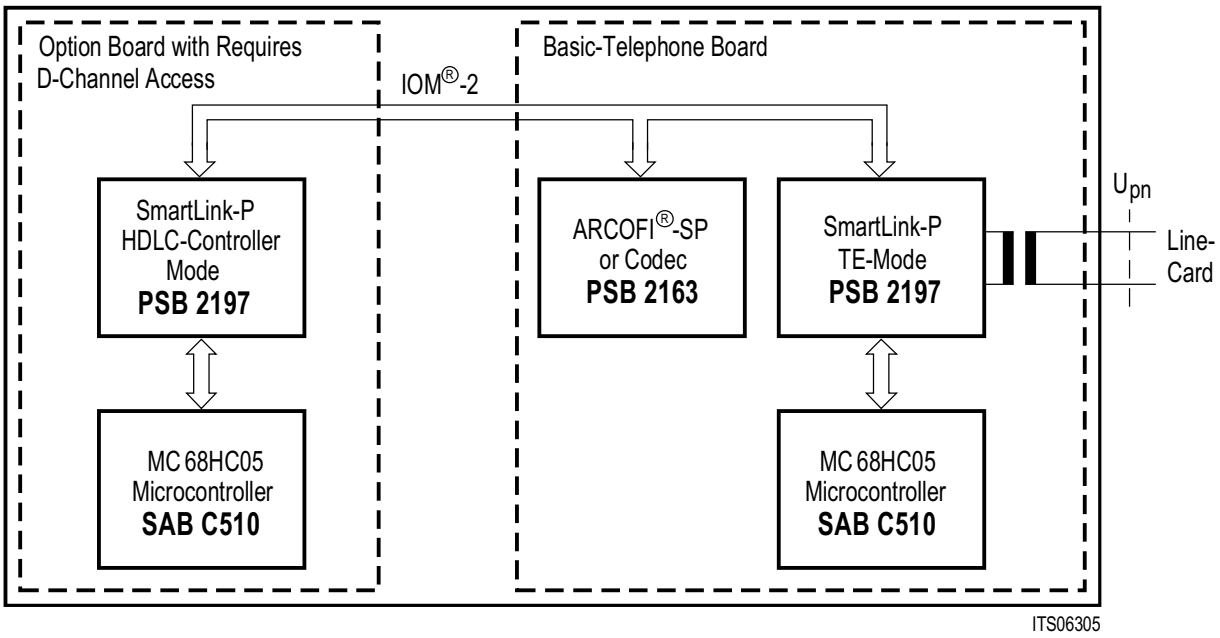


Figure 12
HDLC-Controller on IOM®-2 Extensions

2 Functional Description

Selection between TE-, TR-Mode and HDLC-Controller Mode

The selection between the three operating modes is done via the combination of TR/$\overline{\text{TE}}$-input and PWO/Ring/Mode input.

If TR/$\overline{\text{TE}}$ is connected to V_{SS} (GND), the terminal equipment mode is selected. PWO/Ring/Mode operates as output providing the LCD-contrast or ringing signal.

If TR/$\overline{\text{TE}}$ is connected to V_{DD} (+ 5 V), the PWO/Ring/Mode input selects between TR-mode (‘0’) and HDLC-controller mode (‘1’).

The TR-mode remains as a stand-alone function with the requirement that $\overline{\text{CS}}$ must be connected to V_{DD} and MOSI should be connected to V_{SS}.

If the HDLC-controller mode is selected, the U_{pn}-state machine must reach a defined reset state. Therefore it is necessary to provide a clock signal to XTAL1 which is active during reset and remains active at least 80 clock periods after reset. It is recommended to connect the IOM-2 DCL-signal to XTAL1.

2.1 Terminal Equipment (TE) Mode

2.1.1 General Functions and Device Architecture (TE-mode)

Figure 13 depicts the detailed architecture of the PSB 2197 SmartLink-P in TE-mode:

- U_{pn}-interface transceiver, functionally fully compatible to both PEB 2095 IBC and PEB 2096 OCTAT-P, also features the terminal repeater mode
- Serial control port
- Reset and microcontroller clock generation
- HDLC-controller with 2×4 byte FIFOs per direction
- IOM-2 interface for terminal application
- MUTE function
- B-channel loop on IOM-2
- Pulse width modulator for LCD-contrast control or ring tone generation
- Watchdog timer

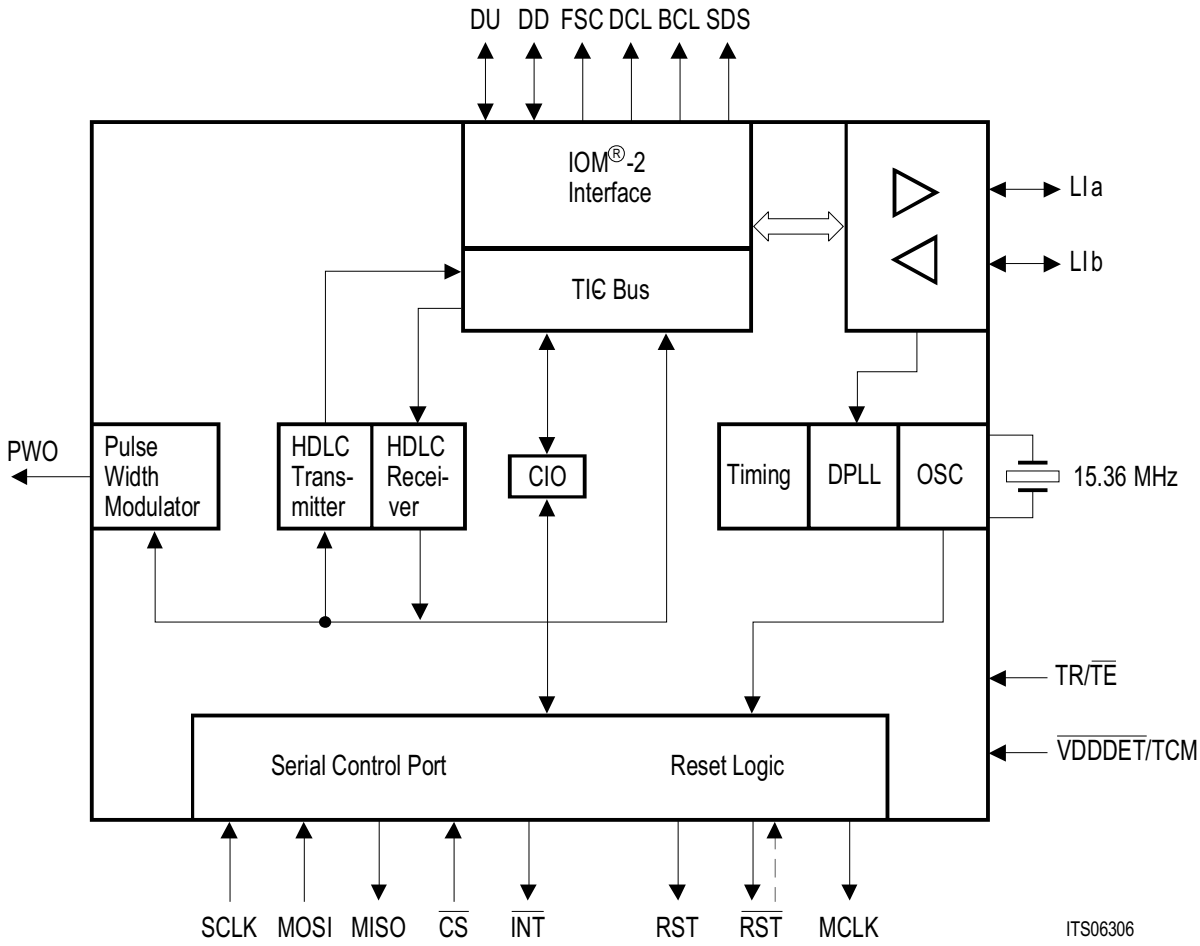


Figure 13
Device Architecture of the SmartLink in TE-Mode

2.1.2 Clock Generation (TE-Mode)

In TE-mode, the oscillator is used to generate a 15.36-MHz clock signal. This signal is used by the DPLL to synchronize the IOM-2 clocks to the received U_{pn}-frames. The oscillator clock is divided by 2 to generate a 7.68-MHz clock which drives the remaining functions. The prescaler for the microcontroller clock divides the 7.68-MHz clock by 1, 2, 4 or 8. The pulse width modulator and the ring tone generator receive their clock signal from a divider which generates a 128-kHz and 32-kHz signal. The later signal is also used to drive the reset/watchdog counter. Note that only the IOM-2 clock signals (FSC, DCL, BCL) may be stopped during the power-down state. The oscillator and the other modules remain active all the time.

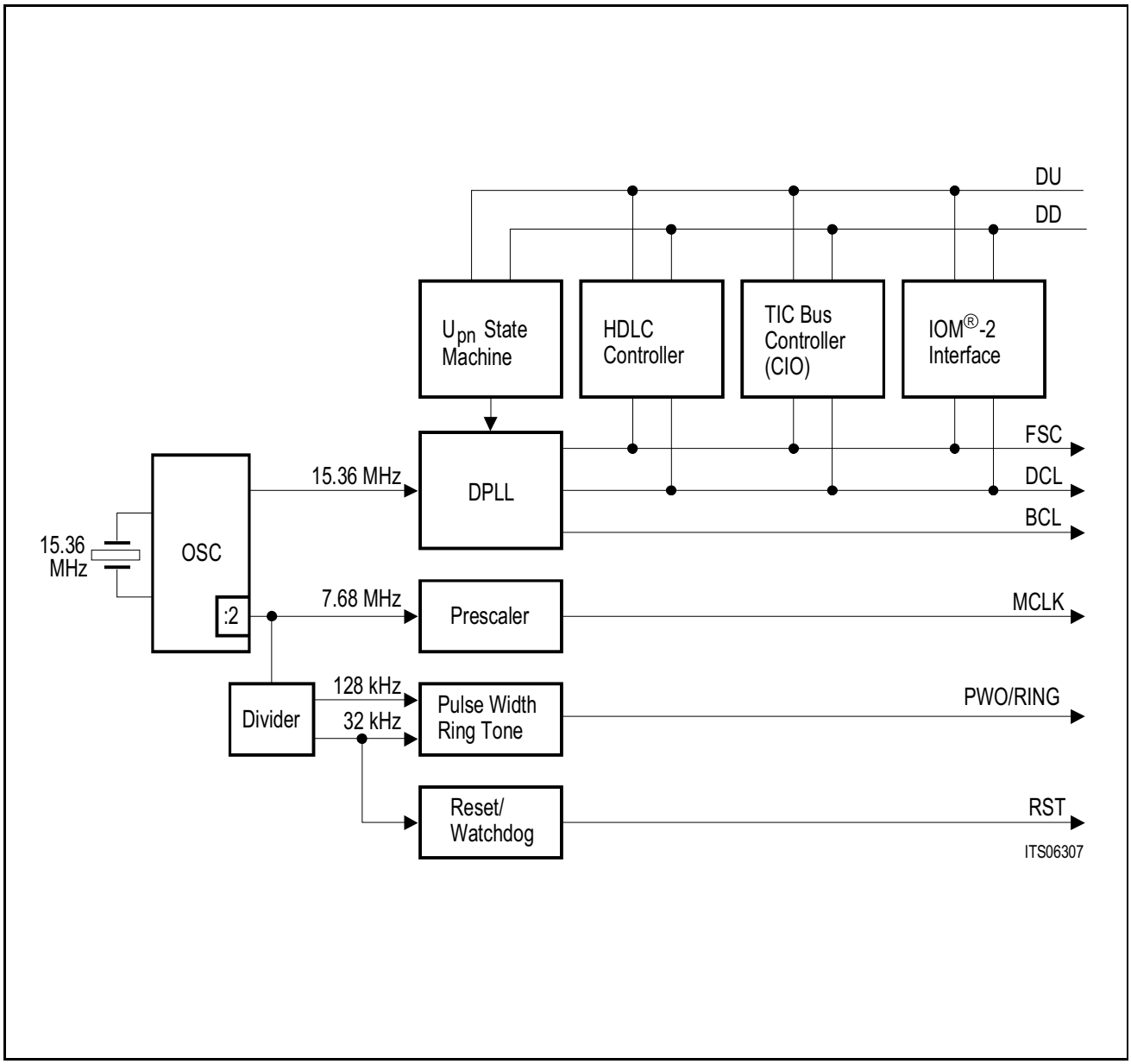


Figure 14
Clock Generation in TE-Mode

2.1.3 Interfaces (TE-Mode)

The PSB 2197 SmartLink-P serves four interfaces in TE-mode:

- Serial microcontroller interface for higher layer functions incl. reset and microcontroller clock generation
- IOM-2 interface: between layer-1 and layer-2 and as a universal backplane for terminals
- U_{pn}-interface towards the two-wire subscriber line
- Pulse width modulator/Ringing output

2.1.3.1 Microcontroller Interface

The SmartLink-P provides a serial control interface which is compatible to the SPI-interface of Motorola or Siemens C510 family of microcontrollers.

Serial Control Interface

The SmartLink-P is programmable via a serial control interface. It provides access to the D-channel FIFOs as well as global control/status registers. It consists of 5 lines:
SCLK, MOSI, MISO, $\overline{CS}$, $\overline{INT}$.

$\overline{CS}$ is used to start a serial access to the SmartLink-P registers: Following a falling edge on $\overline{CS}$, data is transmitted in groups of eight bits until the $\overline{CS}$-line becomes inactive.

The data transfer is synchronized by the SCLK-input. MISO changes with the falling edge of SCLK while the contents of MOSI is latched on the rising edge of SCLK. Data is transferred with the MSB first and LSB last.

The structure of the serial control interface is designed to provide a fast full duplex data transfer.

Two control/status bytes are transferred followed by the data of the HDLC FIFOs. Two additional control bytes can be transferred on request.

Figure 15 shows the timing of a serial control interface transfer.

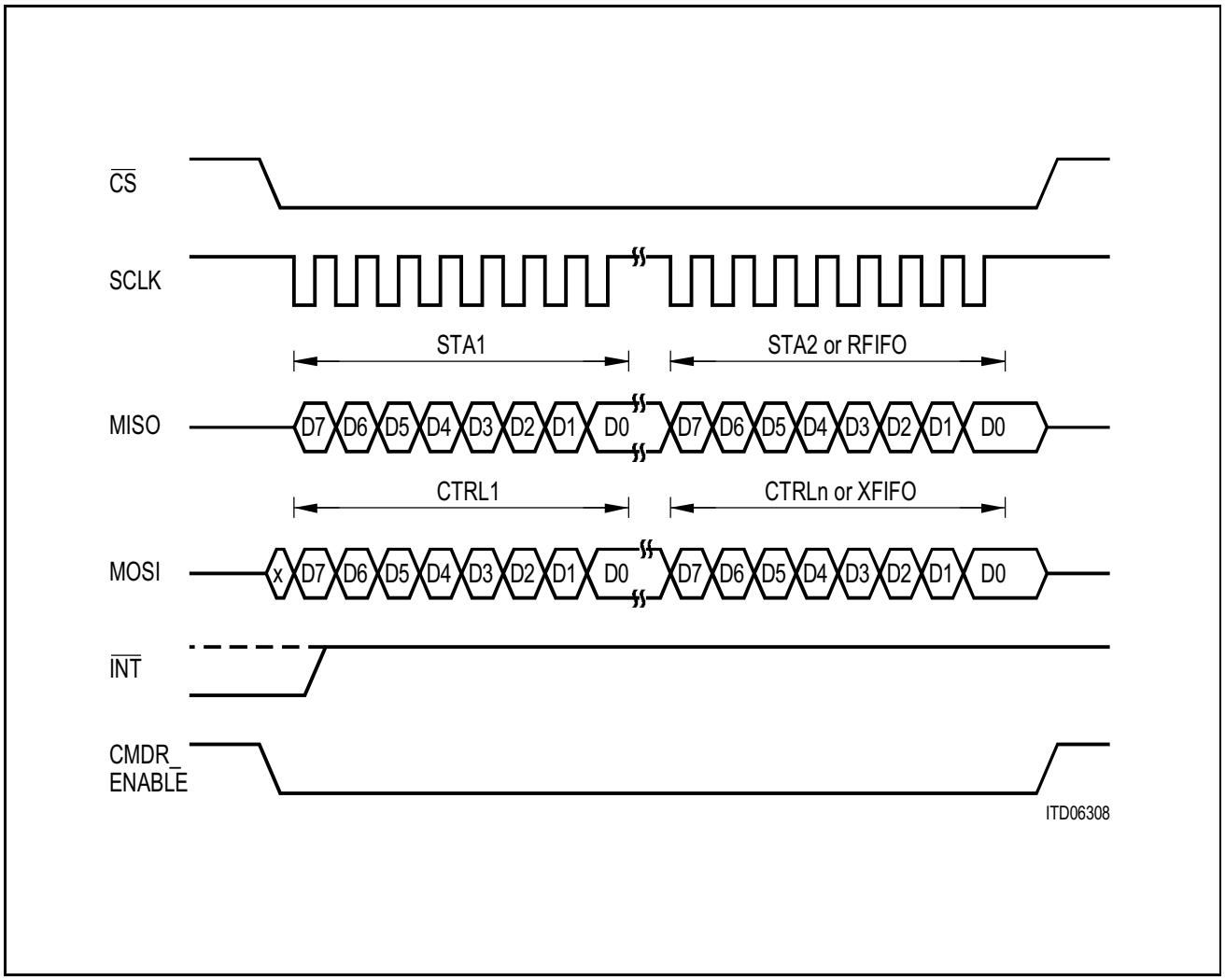


Figure 15
Serial Control Interface Timing

The serial control port outputs a status byte (STA1) while the first control byte (CTRL1) is received. This status byte informs whether D-channel information follows and about the transmitter status. Following this byte a second status byte (STA2) is transmitted while the second control byte (CTRL2) is received. Following these two bytes, FIFO-data or additional control bytes may be transmitted.

The contents of the RFIFO is transmitted if a receive FIFO-status bit was set (RPF, RME) until a receiver command (RMC, RHR, RMD) has been received. After four bytes have been read, the SmartLink continues to transmit RFIFO data as long as transfers are made (as long as $\overline{CS}$ is low and clocks are transferred). The contents of the RFIFO will be repeated after 4 bytes. A new FIFO-access continues with the next byte.

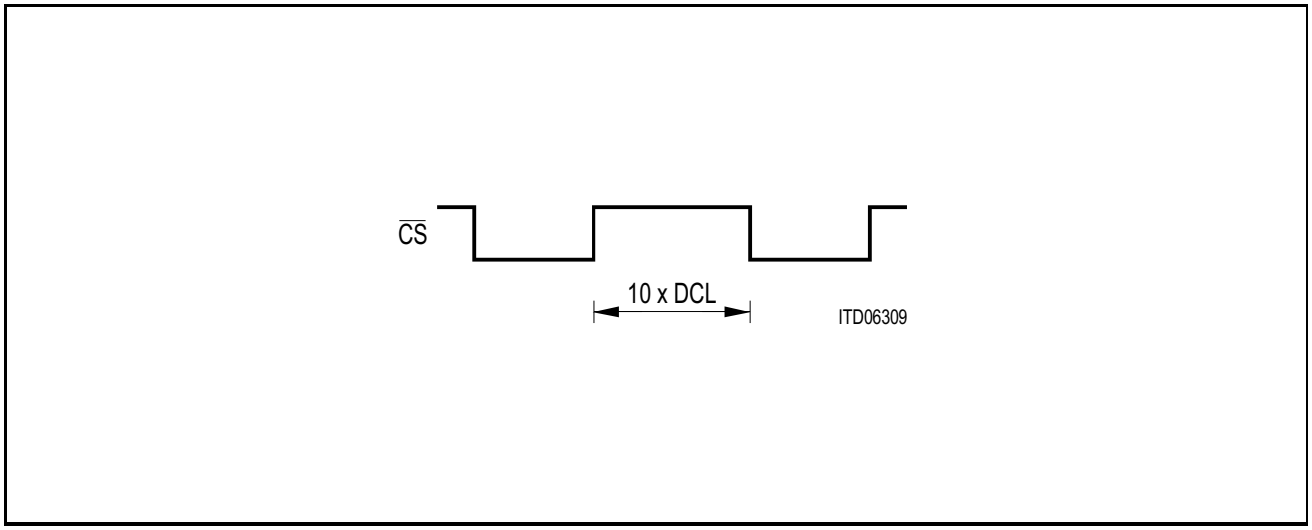
The CTRL2 byte specifies the number of bytes which have to be transferred into the XFIFO in receive direction. Additional data bytes will be ignored.

During transfer of CTRL3 and CTRL4, RFIFO data will not be output.

The access to the serial control interface may be stopped at any time by setting the $\overline{CS}$-input to '1'. If this happens in the middle of a RFIFO-byte, the information of that byte will be lost. In receive direction, the contents of the shift register will not be written into the XFIFO or the proper register.

If the access is stopped during the transfer of RFIFO-data, the SmartLink will output the remaining number of bytes in the next access, but no RFIFO-status bit will be set. Thus, the microcontroller has to monitor the number of transferred bytes.

A minimum interval of 10 DCL clock periods (6.5 µs) is necessary between serial accesses (rising edge of previous access until falling edge of next access). This time is required to perform the commands entered in the CTRL2-register correctly.



An earlier access may result in an incorrect execution of the previous CTRL2-commands.

Figure 16 shows some examples of the data transfer over the serial control interface.

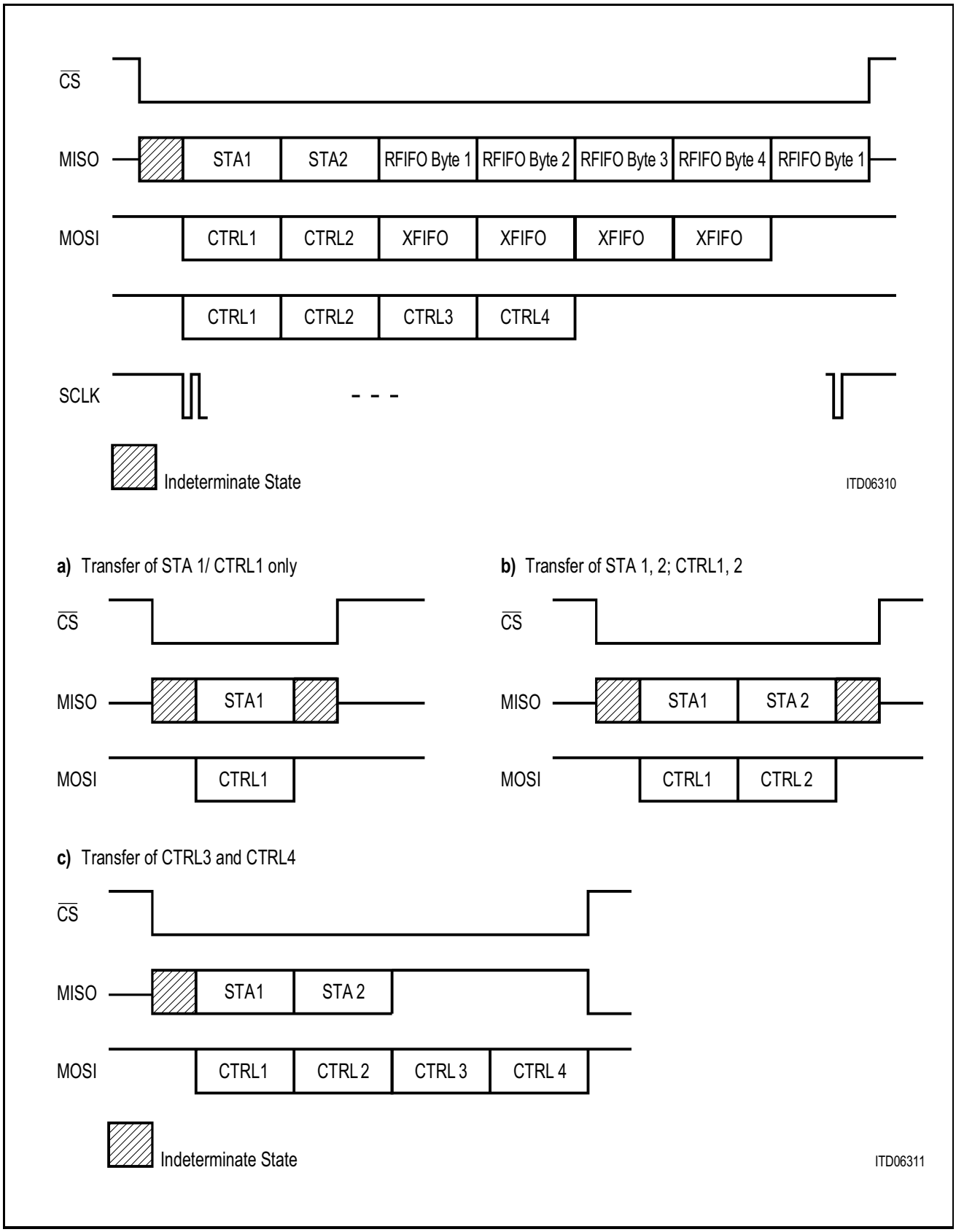


Figure 16
Examples of SCI-Transfers

Figure 17 shows an example how the SmartLink-P is interfaced to a Siemens SAB C510 family of microcontrollers or a Motorola MC68HC05 microcontroller.

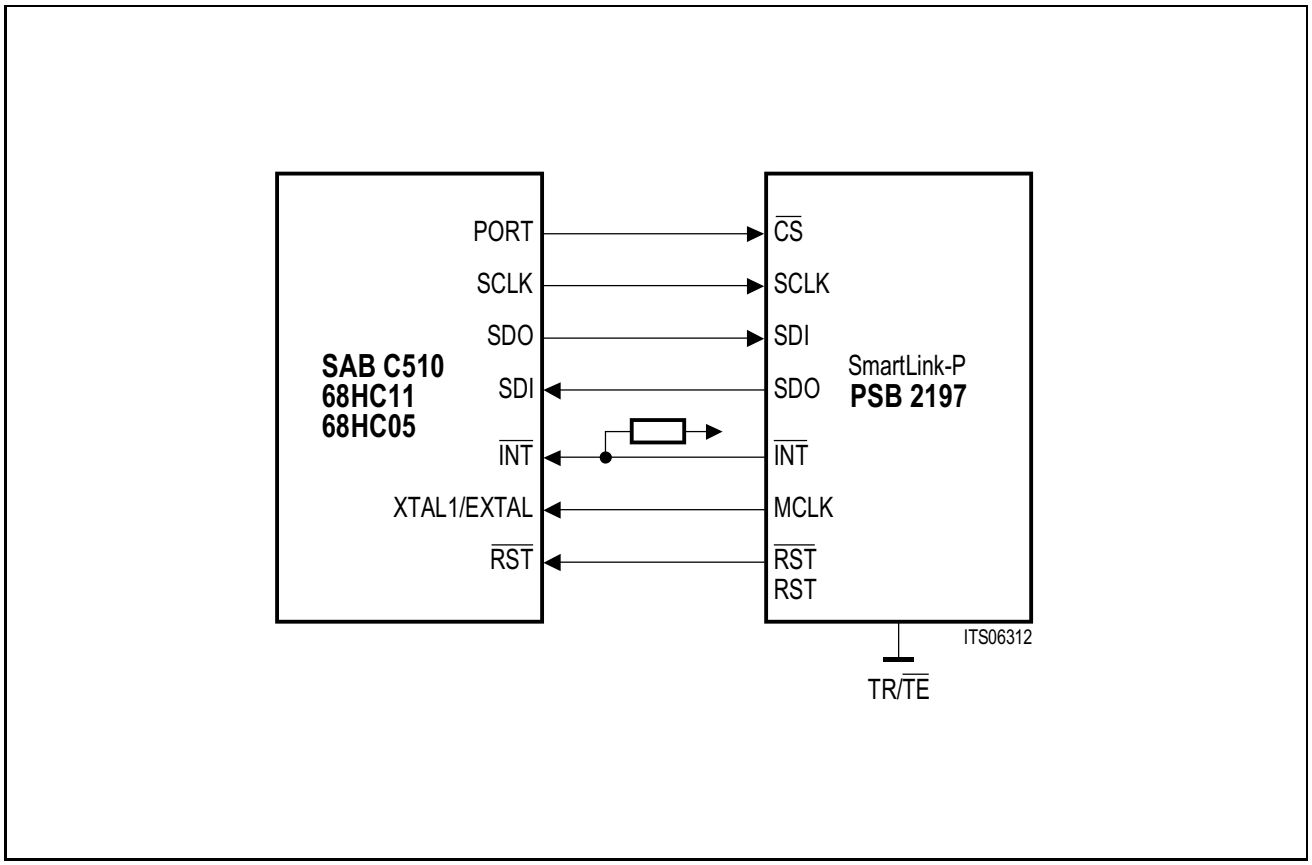


Figure 17
Interfacing the SmartLink-P to a Siemens SAB C510x or Motorola Microprocessor

Microprocessor Clock Output

The microprocessor clock is provided by the MCLK-output. Four clock rates are provided by a programmable prescaler. These are 7.68 MHz, 3.84 MHz, 1.92 MHz, 0.96 MHz. Switching between the clock rates is based on the lowest frequency and realized without spikes.

The value after reset is 3.84 MHz.

The clock rate is changed after $\overline{CS}$ becomes inactive.

Interrupt Output

The interrupt output is an open drain output. The $\overline{INT}$-line can be activated at any time. The interrupt output is masked while $\overline{CS}$ is active. Nevertheless, the interrupt request itself will only be cleared if STA1 or STA2 (in case of C/I-change) is read (2).

If $\overline{CS}$ becomes active and STA1 is not read during this access, $\overline{INT}$ becomes active again after $\overline{CS}$ is turned high (1).

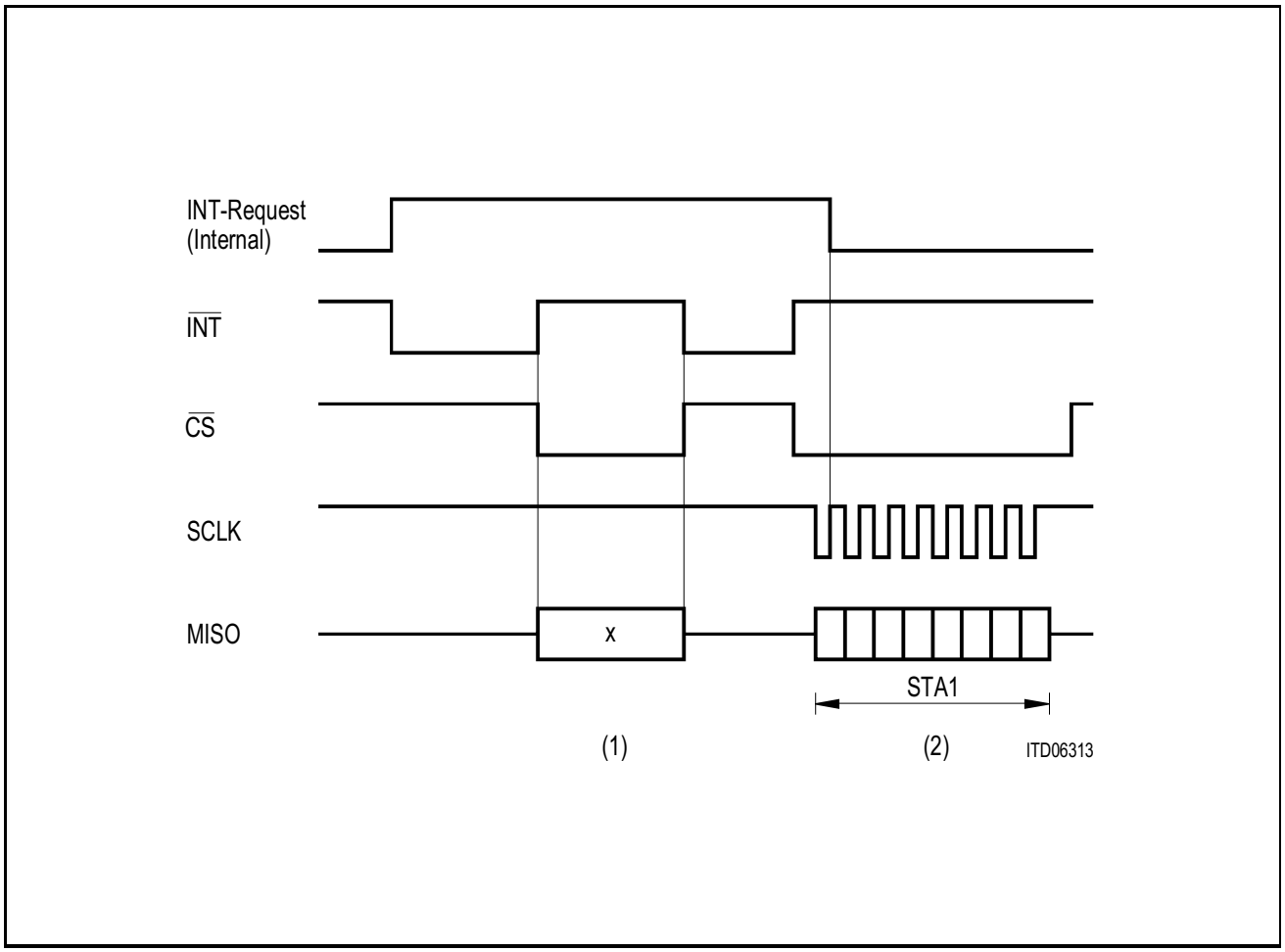


Figure 18
Interrupt Output

Reset Logic

The SmartLink in provides two reset outputs (RST, $\overline{\text{RST}}$) if the undervoltage detection is active. An alternative mode selects $\overline{\text{RST}}$ as input while RST outputs the inverse of $\overline{\text{RST}}$. The undervoltage detection is not active in this mode.

Additionally, a watchdog timer is included which is started by a particular sequence. If it underruns, a reset signal is generated and some of the internal registers are reset.

Undervoltage Detection

During power-up, the reset output is active until the threshold voltage of V_{HH} has been reached. After that, a period of t_r is counted until the reset output becomes inactive. It stays inactive until the supply voltage drops below threshold level V_{HL}.

While the supply voltage is below the thresholds, the microcontroller clock MCLK is stopped and the MCLK-output remains low. If the supply voltage falls below threshold V_{HL}, the clock is stopped immediately which may result in a shorter high period of the clock signal.

For V_{HL} and the hysteresis between V_{HL} and V_{HH} the following values are specified.

Parameter	Limit Values		Unit
	min.	max.	
V_{HL}	4.2	4.4	V
Hysteresis ($V_{HH} - V_{HL}$)	50	230	mV

t_r has a value of 1792 periods of the internal 32-kHz clock which is equal to 56 ms. The minimum period (t_{min}) for the undervoltage detection is at maximum 11 µs. The delay (t_d) after threshold voltages have been passed is maximum 1 µs.

During power-up, the reset pulse may be extended due to the oscillator start until a stable 15.36-MHz clock is achieved.

Figure 19 shows the undervoltage control timing.

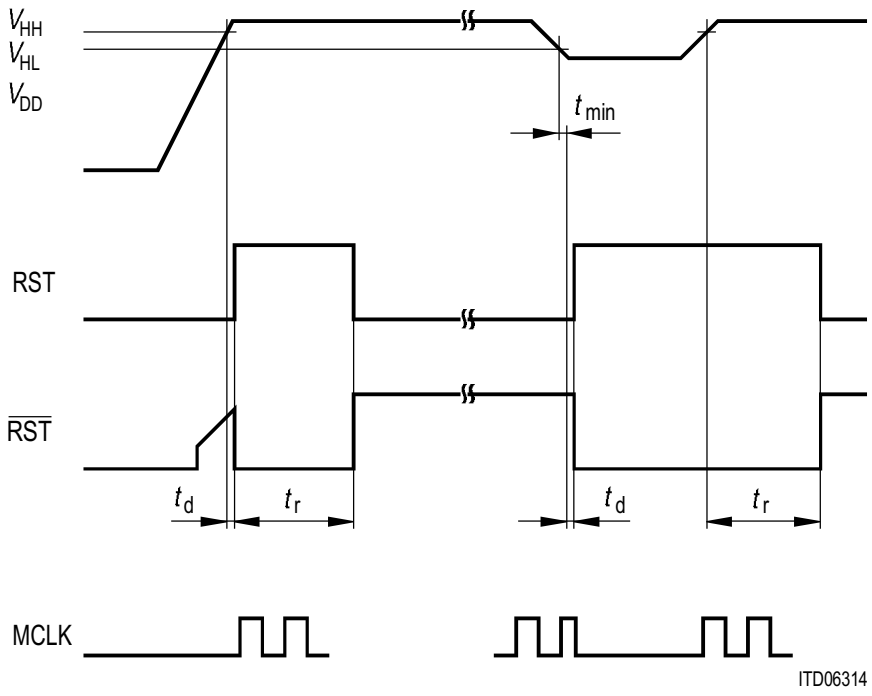


Figure 19
Undervoltage Control Timing

Watchdog Timer

The counter which is used for the reset generation can be used as watchdog timer. Once the power detection reset has been elapsed, the counter is disabled.

It can be enabled as watchdog timer with the first ‘10’ sequence of the WTC1- and WTC2-bits. Once enabled, the software has to program ‘01’, ‘10’ sequences into the WTC1-, WTC2-bits each within 56 ms. If the next sequence doesn’t occur within this period, a reset pulse is generated at the reset output which has a width of 56 ms.

The watchdog reset will only effect the CTRL3-register to reset the SDS-bits so that SDS and BCL become low. The watchdog timer will also reset the CTRL1-register (PW5-0 bits, PRE1, 0) and the LCRI-bit so that the PWO/Ring output becomes low.

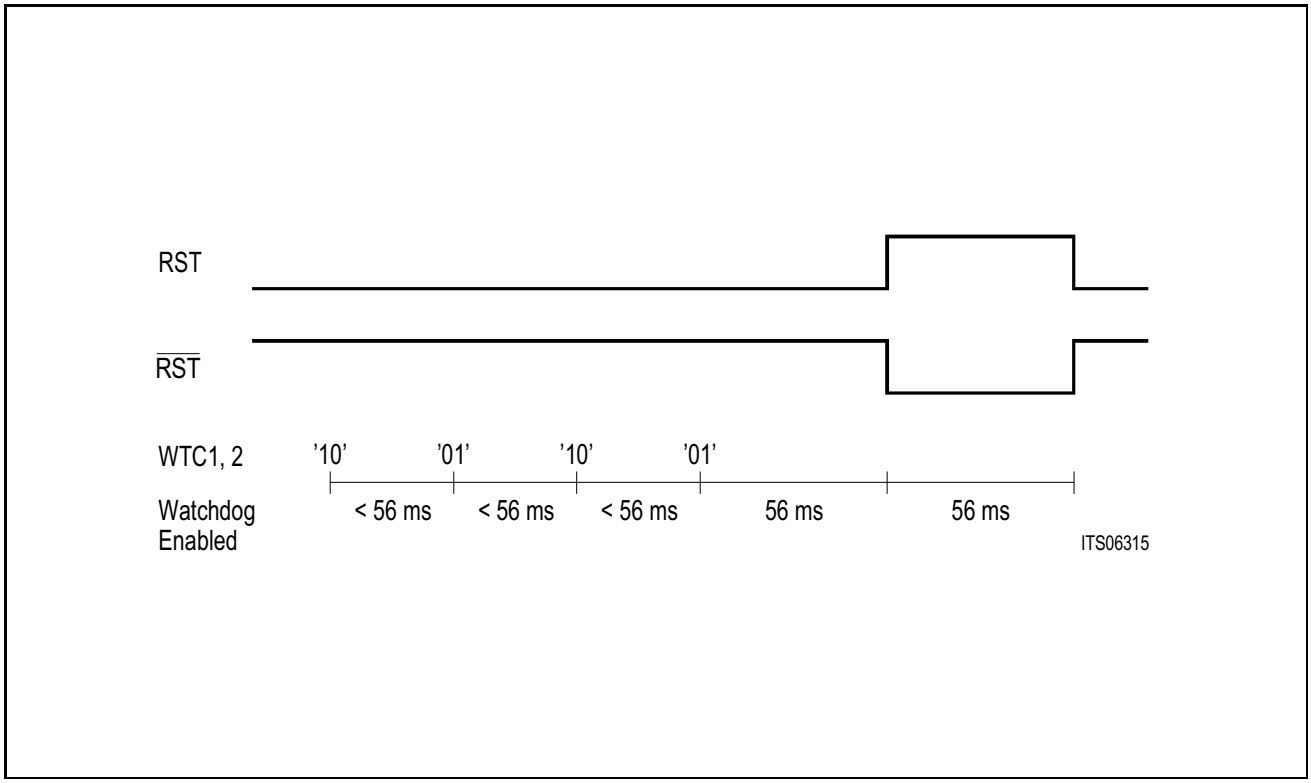


Figure 20
Watchdog Operation

IOM®-Clocks Signals during Reset

The undervoltage detection generates internally a short reset pulse which is used to reset the internal registers and to trigger the 56 ms counter. After the short internal pulse is released, the U_{pn}-transceiver is reset. As a result, IOM-clocks are generated at the begin of the 56 ms external reset pulse and last for 11 IOM-frames (1.375 ms). After that, the IOM-clocks are stopped if the U_{pn}-interface remains deactivated. Generation of IOM-clocks is started after the SPU-bit is set in CTRL4 or if an external device requests IOM-clocks by pulling the data upstream (DU) line low. They are also started if an activation of the U_{pn}-interface is triggered by the line card or terminal repeater.

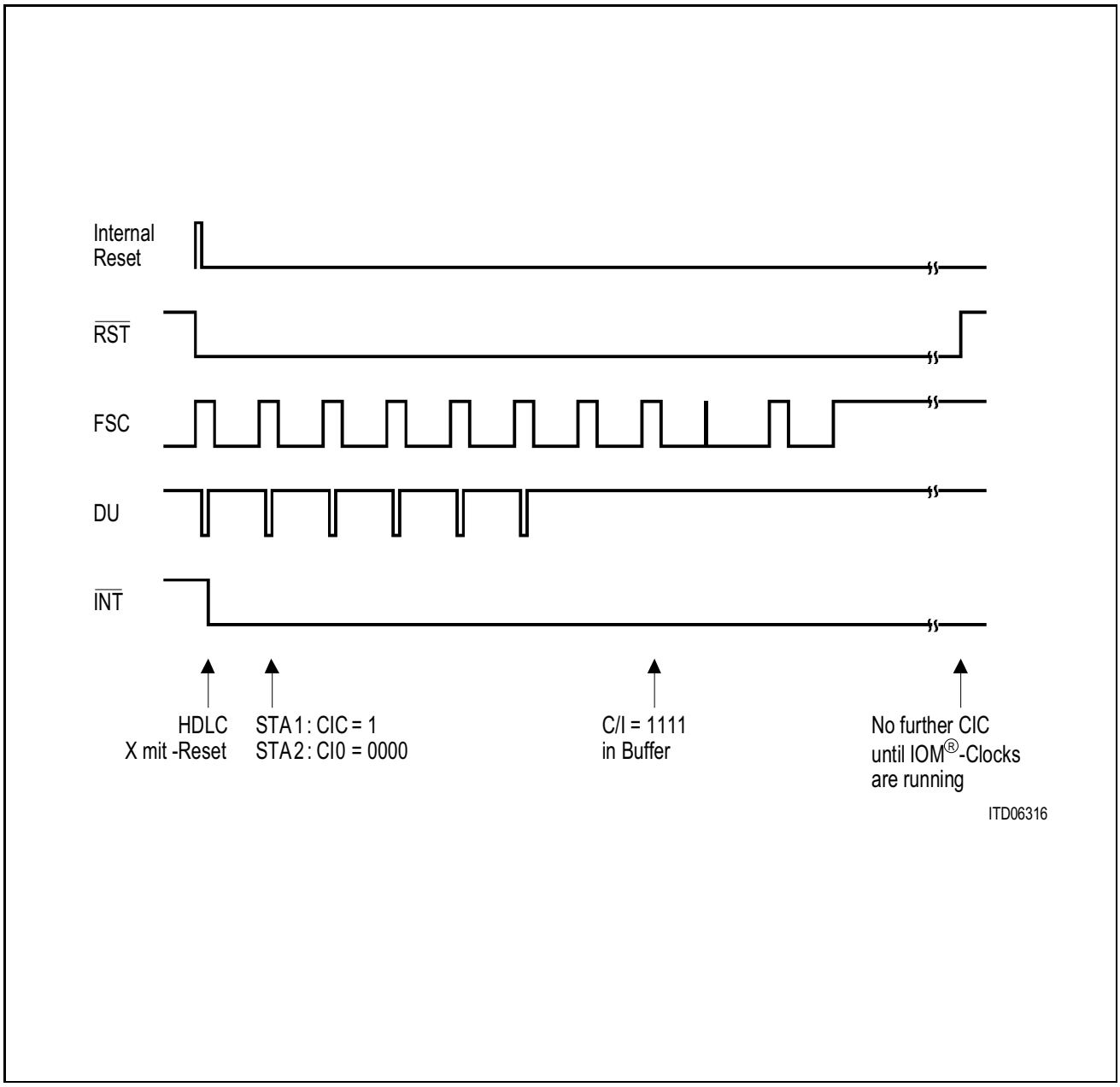


Figure 21
IOM®-Clocks Signals during Reset

The CIC-bit in the STA1-register is set when the microcontroller reads the STA1-register for the first time because the U_{pn}-transceiver outputs a 'DR' indication when it is reset. The 'DC' C/I-indication is stored in the C/I-buffer register. The software, after reading the STA1- and STA2-register will not get another CIC-status change unless the IOM-clocks are running. The value of the buffer register is transferred into the STA2-register only while IOM-clocks are running.

If the SmartLink is configured for an external reset, the IOM-clocks remain running during the reset input is active. IOM-clocks will be stopped after the U_{pn}-transceiver is reset following the end of the reset pulse.

2.1.3.2 IOM®-2 Interface in TE-Mode

The SmartLink-P supports the IOM-2 terminal mode. The interface consists of four lines: FSC, DCL, DD and DU. FSC transfers a frame start signal of which the rising edge indicates the start of an IOM-2 frame (8 kHz). The FSC-signal is generated by the receive DPLL which synchronizes it to the received U_{pn}-frame. The DCL-signal is the clock signal to synchronize the data transfer on both data lines (768 kbit/s frequency is twice the transmission rate (1.536 MHz)). The first rising edge indicates the start of a bit while the second falling edge is used to latch the contents of the data lines. Additionally the BCL- and SDS-signals are provided to connect standard codecs to the SmartLink-P. The BCL (bit clock) provides a clock signal synchronous to the IOM-data at the same data rate. SDS provides a strobe signal which is active high during the B1- or B2- or IC1-channel.

The length of the FSC-signal on the IOM-2 interface will be reduced to one DCL-period every eighth IOM-2 frame. A reduced FSC-signal is generated after a code violation has been received from the U_{pn}-interface.

IOM®-2 Driver

The output driver of the DD- and DU-pins is open drain. The output drivers are active for the selected time-slot bits and remain tristate during the rest of the frame.

IOM®-2 Frame Structure

The principle frame structure of the IOM-2 terminal mode is shown in **figure 22.** The frame is composed of three channels.

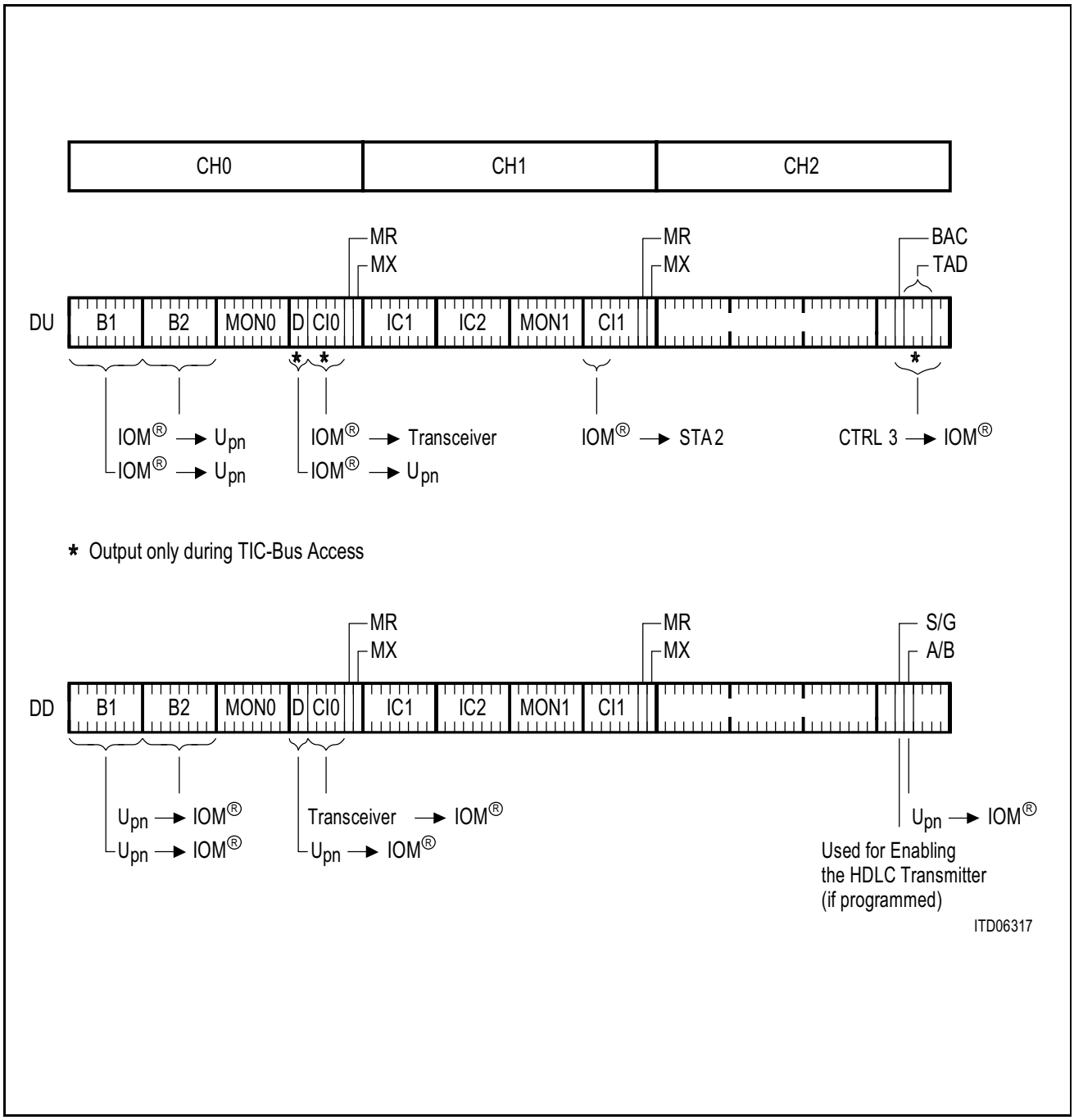


Figure 22
IOM®-2 Terminal Mode

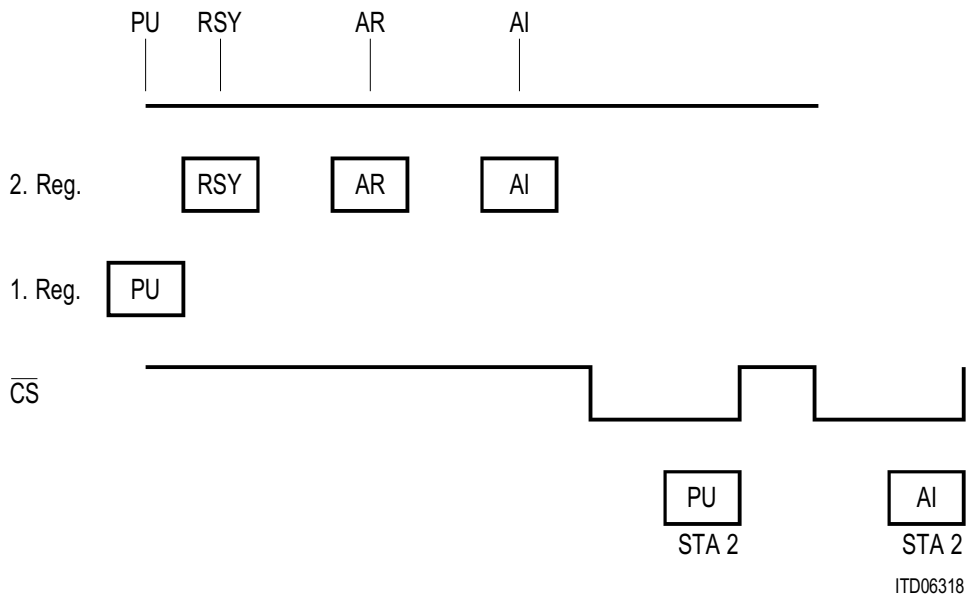
- Channel 0 contains 144 kbit/s of user and signaling data (2B + D) plus a MONITOR and command/indicate channel for control and programming of the layer-1 transceiver.
- Channel 1 contains two 64-kbit/s intercommunication channels plus a MONITOR and command/indicate channel to program or transfer data to other IOM-2 devices.
- Channel 2 is used for the TIC-bus access. Only the command/indicate bits are specified in this channel.

IOM®-2 Time-Slots used by the SmartLink-P

The SmartLink-P accesses a subset of all IOM-2 channels. It provides access to the D-channel, the C/I-channel 0 and to the TIC-bus. The information of the B1-, B2- and D-channel time-slots is forwarded transparently between the IOM-2 interface and the transceiver (in the activated state). Other time-slots (like IC1, IC2, MON0, MON1 with control/status bits) are not influenced by the SmartLink-P. They can be controlled by other devices connected to the IOM-2 interface. The most significant three bits of the C/I-channel 1 are received in the STA2-register.

Command/Indicate 0

C/I-code changes occur at maximum rate of 250 µs (2 × IOM-frames). During activation the following sequence could occur:



If the software is not able to follow each change, it will at least get the first one and the last one. Thus it knows from where it started and about the current status.

Stop/Go Bit

The Stop/Go (S/G) bit can be controlled by the received U_{pn} T-channel to transmit the state of the line card arbiter to the HDLC-controller of the terminal. If selected by the SGE-bit, the HDLC-transmitter evaluates the state of the S/G-bit before and during transmission of an HDLC-frame.

Available/Busy Bit

The AB-bit has been added to the IOM-2 frame for the operation of a S/T-terminal adapter based on the SBCX. Since the SmartLink is not capable of transferring monitor channel data, a masked version of the SBCX was defined which reaches all necessary modes after reset. This part is called PSB 20810.

The terminal needs to know if a PSB 20810 is plugged in to switch the routing of the downstream T-channel correctly.

MUTE Function

The SDS-bits control the data path of the upstream B-channel information. B-channel information may either be transparent (IOM $\rightarrow$ U_{pn}) or disconnected. In the latter state, a constant value of all '1' is transmitted to the U_{pn}-interface instead of the IOM-2 B-channel information. This feature can be used to realize a MUTE function together with a simple codec. The downstream B-channel data is not influenced.

B-Channel Loopback

The information of a B-channel (B1 or B2) received from the U_{pn}-interface can be looped back to the U_{pn}-interface. The selection is done via the SDS2-0 bits.

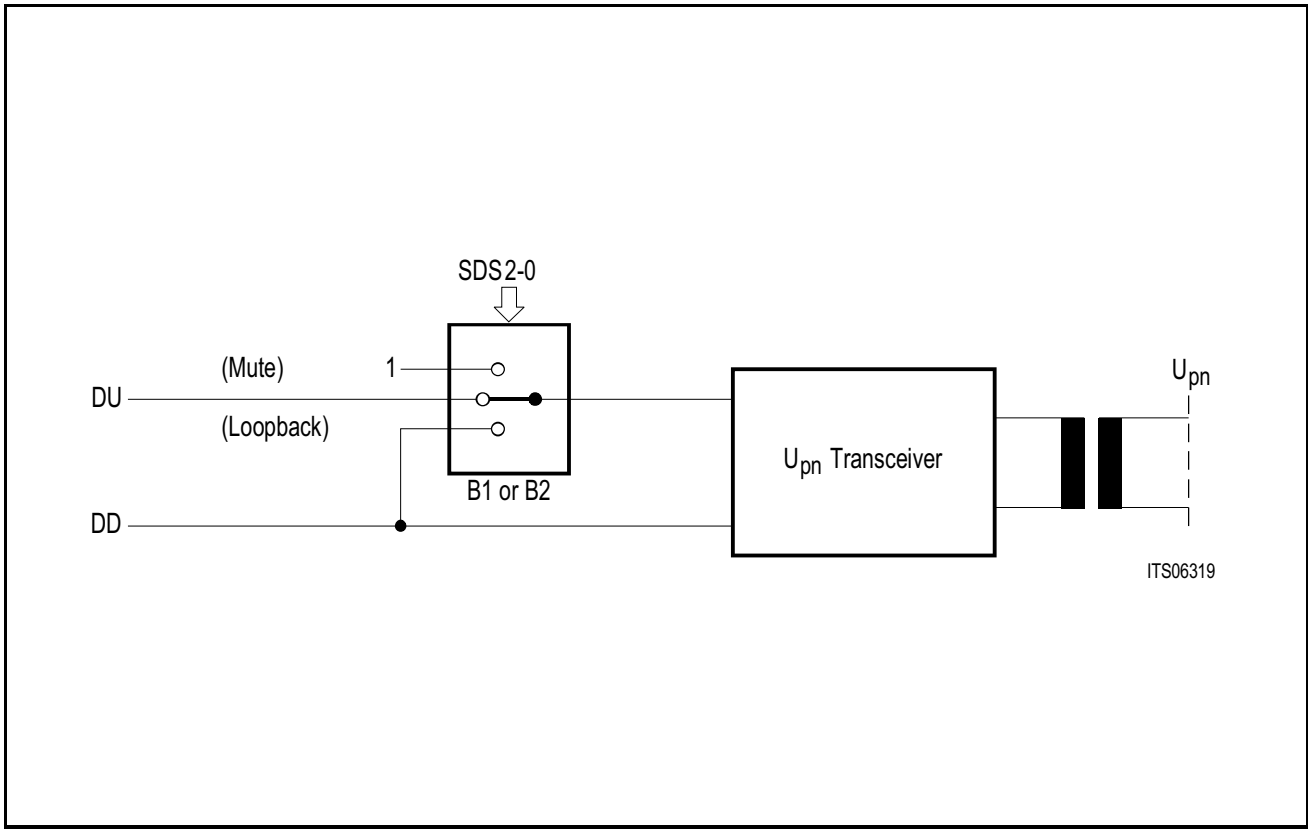


Figure 23
B-Channel Manipulation

2.1.3.3 U_{pn}-Interface

Figure 24 demonstrates the general principles of the U_{pn}-interface communication scheme. A frame transmitted by the exchange (LC) is received by the terminal equipment (TE) after a line propagation delay. The terminal equipment waits the minimum guard time (5.2 µs) while the line clears. It then transmits a frame to the exchange. The exchange will begin a transmission every 250 µs (known as the burst repetition period). However, the time between the reception of a frame from the TE and the beginning of transmission of the next frame by the LC must be greater than the minimum guard time.

Within a burst, the data rate is 384 kbit/s and the 38-bit frame structure is as shown in **figure 24**. The framing bit (LF) is always logical '1'. The frame also contains the user channels (2B + D). Note that the B-channels are scrambled. It can readily be seen that in the 250-µs burst repetition period, 4 D-bits, 16 B1-bits and 16 B2-bits are transferred in each direction. This gives an effective full duplex data rate of 16 kbit/s for the D-channel and 64 kbit/s for each B-channel. The final bit of the frame is called the M-bit.

Four successive M-bits, from four successive U_{pn}-frames, constitute a superframe (**figure 24**). Three signals are carried in this superframe. The superframe is started by a code violation (CV). From this reference, bit 3 of the superframe is the service channel bit (S). The S-channel bit is transmitted once in each direction in every fourth burst repetition period. Hence the duplex S-channel has a data rate of 1 kbit/s. It conveys test loop control information from the LC to the TE and reports of transmission errors from the TE to the LC. Bit 2 and bit 4 of the superframe are the T-bits. Not allocated to a specific function until now (cf PEB 2095 IBC and PEB 20950 ISAC-P) they can be used for D-channel control in conjunction with PEB 20550 ELIC® and PEB 2096 OCTAT-P.

In order to decrease DC-offset voltage on the line after transmission of a CV in the M-bit position, it is allowed to add a DC-balancing bit to the burst. The LC-side transmits this DC-balancing bit, when transmitting INFO 4 and when line characteristics indicate potential decrease in performance.

Note that the guard time in TE is always defined with respect to the M-bit, whereas AMI-coding includes always all bits going in the same direction.

The coding technique used on the U_{pn}-interface is half-bauded AMI-code (i.e. with a 50 % pulse width). A logical '0' corresponds to a neutral level, a logical '1' is coded as alternate positive and negative pulses.

In the terminal repeater mode, no DC-balancing bit will be generated. The loop length of the TR-mode is limited to 100 m.

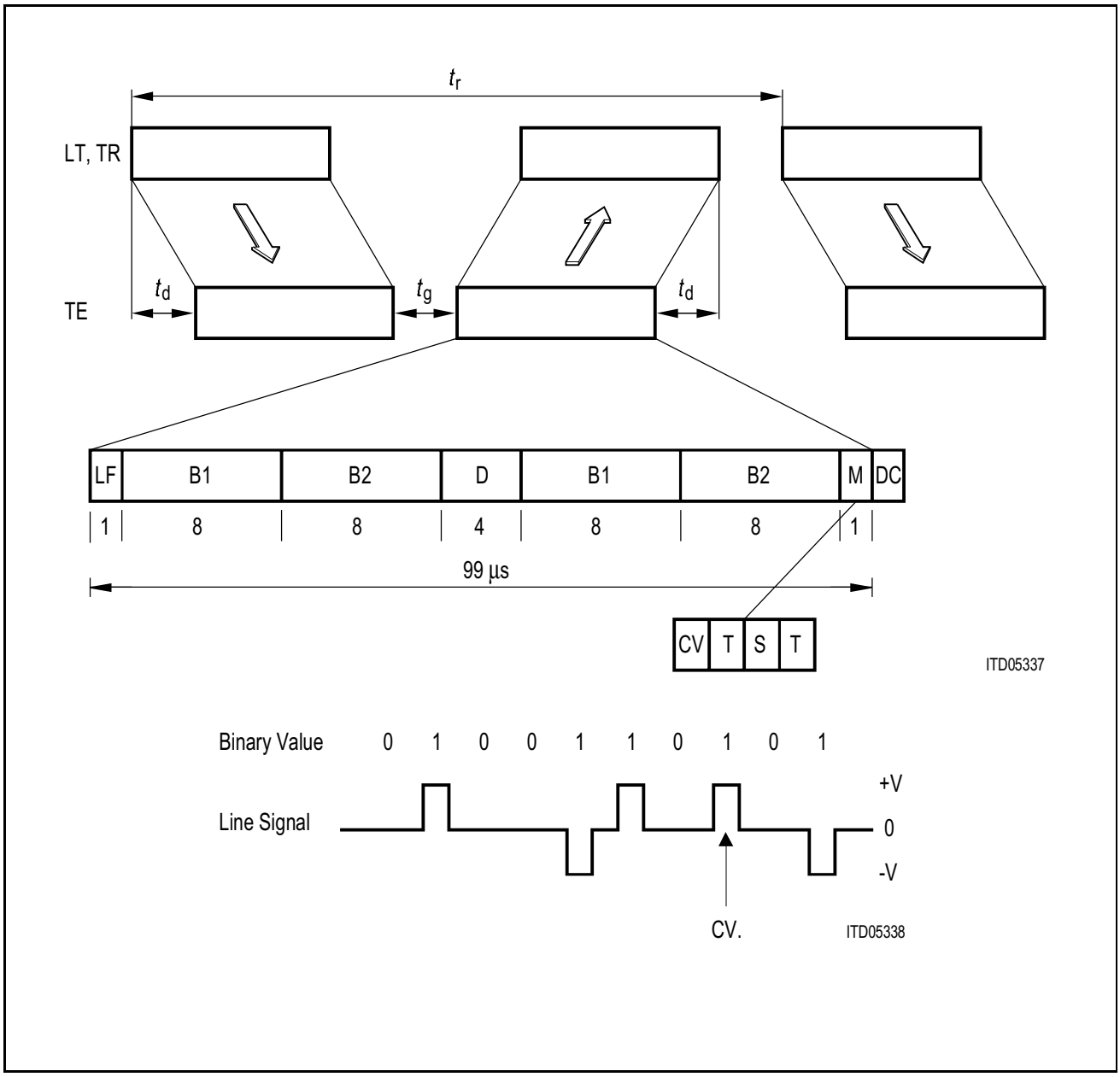


Figure 24
U_{pn}-Interface Structure

Scrambler/Descrambler

B-channel data on the U_{pn}-interface is scrambled to give a flat continuous power density spectrum and to ensure enough pulses are present on the line for a reliable clock extraction to be performed at the downstream end.

The SmartLink-P therefore contains a scrambler and descrambler, in the transmit and receive directions respectively. The basic form of these are illustrated in **figure 25**.

The form is in accordance with the CCITT V.27 scrambler/descrambler and contains supervisory circuitry which ensures no periodic patterns appear on the line.

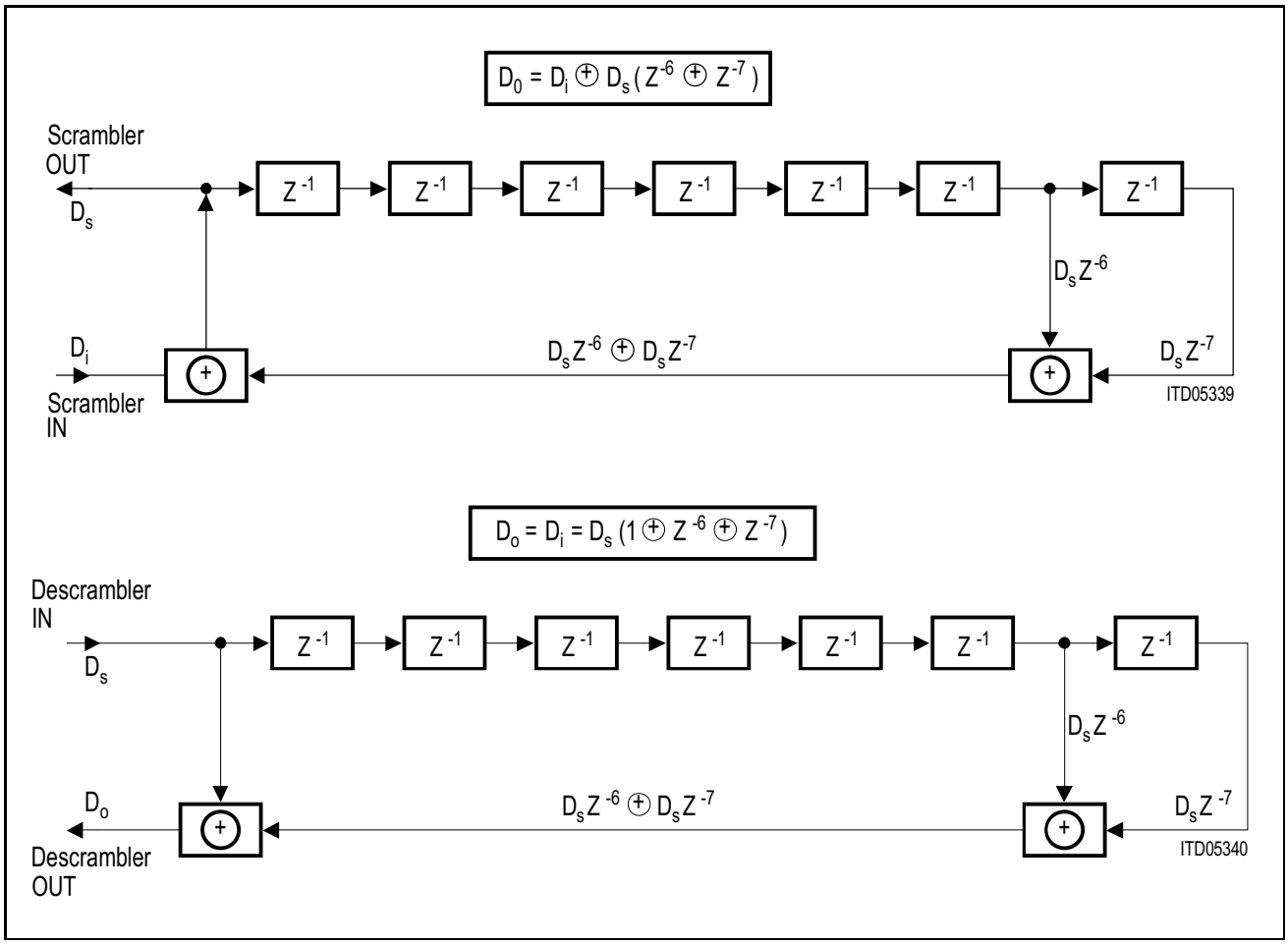


Figure 25
Scrambler/Descrambler

Info Structure on the U_{pn}-Interface

The signals controlling the internal state machine on the U_{pn}-interface are called infos. In effect these pass information regarding the status of the sending U_{pn}-transceiver to the other end of the line. They are based upon the same format as the U_{pn}-interface frames and their precise form is shown in **table 1**.

When the line is deactivated info 0 is exchanged by the U_{pn}-transceivers at either end of the line. Info 0 effectively means there is no signal sent on the line in either direction.

When the line is activated info 3 upstream and info 4 downstream are continually exchanged. Both info 3 and info 4 are effectively normal U_{pn}-interface data frames containing user data and exchanged in normal burst mode.

Note that the structure of info 1 and info 2 are the same, they only differ in the direction of transmission. Similarily info 3/info 4 and info 1w/info 2w also constitute info pairs. This will be important when considering looped states.

As we will see, the other infos are exchanged during various states which occur between activation and deactivation of the line.

Table 1
U_{pn}-Interface Info Signals

Name	Direction	Description
Info 0	Upstream Downstream	No signal on the line
Info 1w	Upstream	Asynchronous wake signal 2-kHz burst rate F000100010001000100010101010001011111 1 Code violation in the framing bit
Info 1	Upstream	4-kHz burst signal F000100010001000100010101010001011111M[1] DC[2] Code violation in the framing bit
Info 2	Downstream	4-kHz burst signal F000100010001000100010101010001011111M[1] DC[2] Code violation in the framing bit
Info 3	Upstream	4-kHz burst signal No code violation in the framing bit User data in B-, D- and M-channels B-channels scrambled, DC-bit[2] optional
Info 4	Downstream	4-kHz burst signal No code violation in the framing bit User data in B-, D- and M-channels B-channels scrambled, DC-bit[2] optional

Note:

[1] The M-channel superframe is transparent:
S-bits transparent (1-kbit/s channel)
T-bits transparent (2-kbit/s channel)

[2] DC-balancing bit

The following test patterns are also included:

Name	Direction	Description
Info T1	Upstream	Test signal single pulse 2-kHz burst rate 100000000…
Info T2	Upstream	Test signal continuous pulses 192-kHz clock rate 111111111…

U_{pn}-Transceiver

Figure 26 depicts the transceiver architecture and the analog connections of the SmartLink-P. External to the line interface pins LIa and LIb a transformer and external resistors are connected as shown. Note that the internal resistors of the transformer are calculated as zero. The actual values of the external resistors must take into account the real resistor of the chosen transformer.

The receiver section consists of an amplifier followed by a peak detector controlling the thresholds of the comparators. In conjunction with a digital oversampling technique the PSB 2197 SmartLink-P covers the electrical requirements of the U_{pn}-interface for loop lengths of up to 4.5 kft on AWG 24 cable and 1.0 km on J-Y(ST) Y $2 \times 2 \times 0.6$ cable.

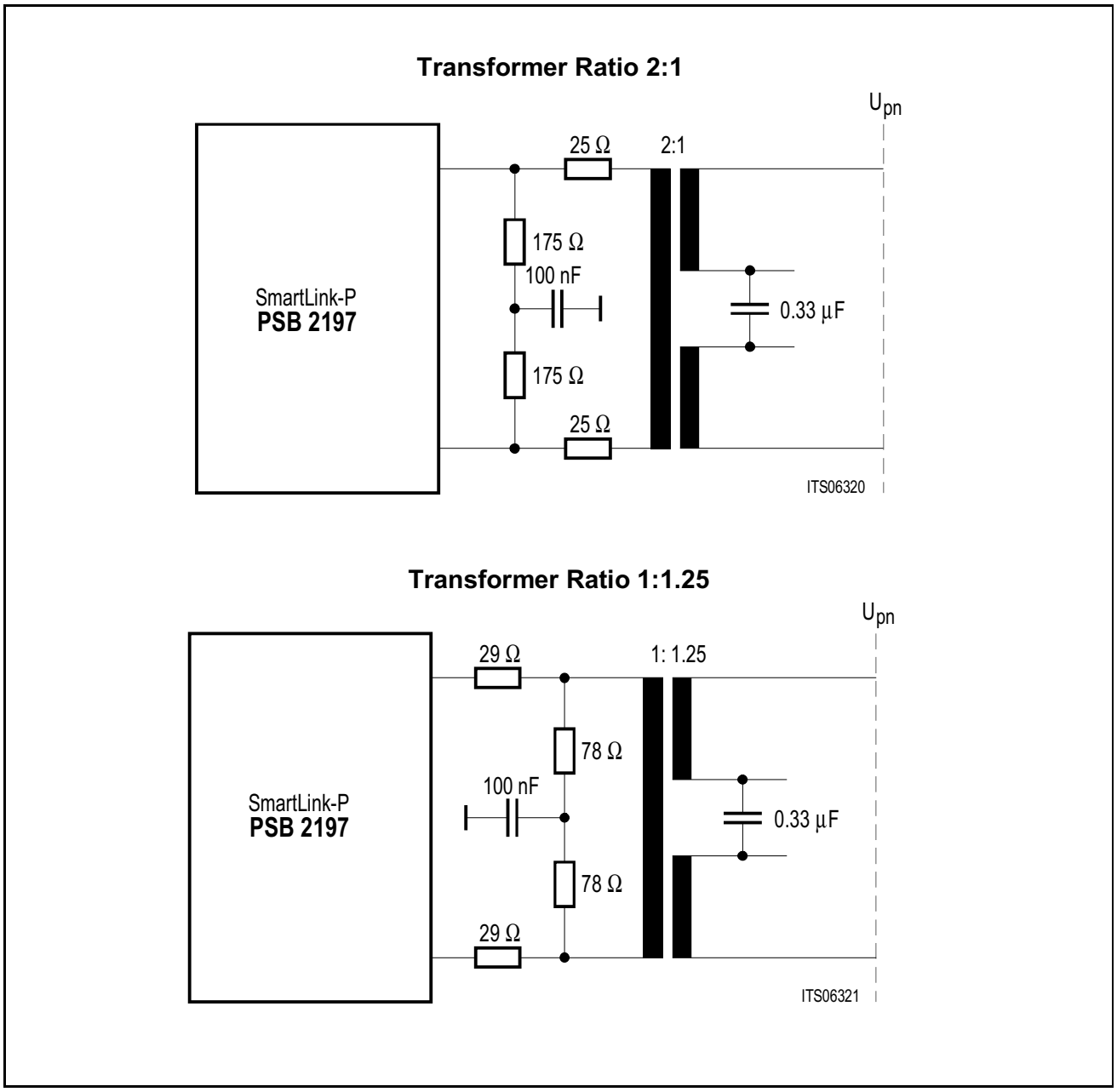


Figure 26
U_{pn}-Transceiver of the SmartLink-P

U_{pn}-Transceiver Timing

The receive PLL uses the 15.36-MHz clock to generate an internal 384-kHz signal which is used to synchronize the PLL to the received U_{pn}-frame. The PLL outputs the FSC-signal as well as the 1.536-MHz double bit clock signal and the 768-kHz bit clock.

The length of the FSC-signal is reduced in the next IOM-2 frame which is started while a U_{pn}-frame is received, after a code violation has been detected. The reduced length of the FSC-signal provides synchronization between the TE- and the TR-transceiver to gain the shortest delays on the U_{pn} T-channel data forwarding.

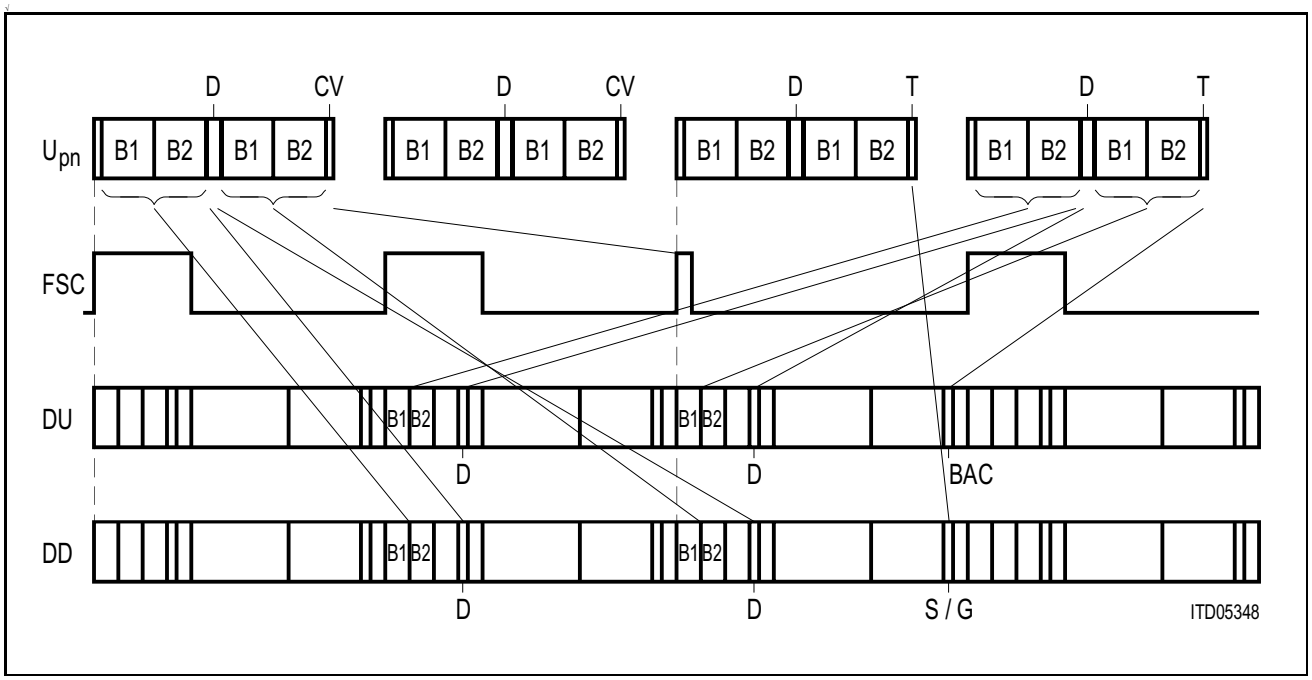


Figure 27
U_{pn}-Transceiver Timing
B1-, B2-Channels

The IOM-interface B-channels are used to convey the two 64-kbit/s user channels in both directions. However, the PSB 2197 SmartLink-P only transfers the data transparently in the activated state (incl. analog loop activated) while the data are set to '1' in any non activated state (cf. state descriptions).

D-Channel

Similar to the B-channels the layer-1 (U_{pn}) part of the PSB 2197 SmartLink-P transfers the D-channel transparently in both directions in the activated state.

T-Bit Transfer

In TE-mode the layer-1 (U_{pn}) part of the PSB 2197 SmartLink-P conveys the T-bit position of the U_{pn}-interface to either the S/G-bit position or the A/B-bit position according to the register programming. The exact bit polarities are as follows:

Downstream ($U_{pn} \rightarrow$ IOM®)

T-to A/B-mapping (CTRL3: TCM = 1):

T = 0: A/B = 0 S/G = 1 blocked
T = 1: A/B = 1 S/G = 1 available

T-to S/G-mapping (CTRL3: TCM = 0):

T = 0: A/B = 1 S/G = 1 blocked
T = 1: A/B = 1 S/G = 0 available

Upstream (IOM® → U_{pn})

The T-channel in upstream direction is controlled by the BAC-bit of the IOM-2 interface. The T-channel transmits the inverse of the BAC-bit.

Special care is taken so that the slave terminal will only send one HDLC-frame until the TIC-bus of the master IOM-2 interface is release. This is achieved by a circuitry which latches the BAC-state of '1' until at least one T-bit has been transmitted with the value of '0' which releases the TIC-bus of the master IOM-2 interface.

BAC to T-mapping:

BAC = 1	T = 0	no D-channel request
BAC = 0	T = 1	D-channel request

Control of the U_{pn}-Transceiver

An incorporated finite state machine controls the activation/deactivation procedures and communications with the layer-2 section via the IOM-Command/Indicate (CI) channel 0.

Diagnostics Functions

Two test loops allow the local or the remote test of the transceiver function.

Test loop 3 is a local loop which loops the transmit data of the transmitter to its receiver. The information of the IOM-2 upstream B- and D-channels is looped back to the downstream B- and D-channels. The M-bit is also transparent which means that the state of the BAC-bit is looped back to the S/G- or AB-bit.

Test loop 2 is activated by the U_{pn}-interface and loops the received data back to the U_{pn}-interface. The D-channel information received from the line card is transparently forwarded to the downstream IOM-2 D-channel.

The downstream B-channel information on IOM-2 is fixed to 'FF'$_H$ while test loop 2 is active.

2.1.4 D-Channel-Arbitration in TE-Mode

The SmartLink-P supports different kinds of D-channel arbitration in order to share the upstream D-channel by several communication controllers and to allocate the D-channel from the U_{pn}-interface.

The following functions are performed depending on the register settings:

– Allocation of the upstream D-channel bits on the IOM-2 interface via the TIC-bus.
– Control of the HDLC-transmitter by the stop/go bit.

TIC-Bus Access

The terminal IC-bus provides an access mechanism to share the D-channel in upstream direction by several communication controllers (ICC, ISAC, SmartLink) connected to one layer-1 device. The Bus Accessed bit (BAC) is used to indicate that the TIC-bus is currently occupied and other devices have to wait. The different communication controllers use individual TIC-bus addresses in the range of ‘0’ to ‘7’. A collision detection mechanism checks each bit of the TIC-bus address for congestion. Since a ‘0’ has higher priority against a ‘1’, a TIC-bus address of ‘0’ has the highest priority and ‘7’ has the lowest one.

TIC-Bus Access Mechanism

During idle state, the Bus Accessed bit (BAC) is set to ‘1’ and the TIC Bus Address (TBA) is ‘7’. If a communication controller needs access to the D-channel bits, it will check the state of the BAC bit. If BAC is ‘1’ (idle) it will place its TIC-bus address on the TAD2-0 bits. After each bit has been outputted, it checks for collision and stops transmitting if a collision is detected (‘1’ transmitted, ‘0’ detected on the DU-line). If the TIC-bus address has been transmitted successfully, the D-channel and C/I-channel 0 are controlled from the controller in the next frame and the BAC-bit is set to ‘0’. After the TIC-bus access is completed, the TIC-bus returns to the idle state (BAC = ‘1’, TAD = ‘111’) and other devices can gain access.

A device which has detected a collision during the transmission of the TIC-bus address will restart after the BAC-bit becomes idle ‘1’ again. In order to provide access to all controllers, the device which has gained successful access to the TIC-bus will wait for two idle frames before it starts another access.

Note: The SmartLink will also set the BAC-bit if the TIC-bus address of seven (‘111’) is programmed. This is different to the TIC-bus operation of the ICC (PEB 2070) and ICC-based devices (ISAC-S (TE), ISAC-P (TE)).

Stop/Go Bit

The stop/go bit controls the transmitter output of the D-channel HDLC-controller if selected by the SGE-bit. The transmitter is active, as long as the stop/go bit indicates go (‘0’).

The S/G-bit is checked before a HDLC-frame is started and monitored during the transmission of the HDLC-frame. The HDLC-transmitter aborts the transmission of an HDLC-frame if the S/G-bit becomes ‘Stop’ after the begin of a frame was transmitted. It will output ‘11’ in the D-bits of the IOM-frame beginning with the following IOM-frame after S/G becomes ‘Stop’ until ‘Go’ is indicated. The evaluation of the S/G-bit must be enabled by the CTRL3:SGE-bit.

The stop/go bit can be controlled by the downstream T-bit which indicates the receive capability of the line card or by the PSB 20810 in case a S/T-interface adapter is plugged onto the IOM-2 interface.

HDLC-Controller Access Modes

The access mode of the D-channel HDLC-controller is programmable. It can ignore the TIC-bus, use the TIC-bus to gain access and evaluate the S/G-bit.

Table 2 shows the possible combinations.

Table 2
HDLC-Controller Access Modes

TBU	SGE	TIC-Bus Access	S/G-Evaluation	Application
1	0	Yes	No	TIC-bus access without S/G-bit evaluation
1	1	Yes	Yes	TIC-bus access with S/G-bit evaluation
0	0	No	No	Permanent D-channel access without S/G-bit evaluation
0	1	No	Yes	Permanent D-channel access with S/G-bit evaluation

If the HDLC-controller is set to a mode where the S/G-bit is evaluated, the transmission is started if the S/G-bit becomes go (‘0’) and stopped if the S/G-bit becomes stop (‘1’).

If the D-channel becomes not available before the final bit of the closing flag has been sent, the transmission is aborted. In case the collision occurred during the first XFIFO contents, the frame is automatically retransmitted. If the first XFIFO contents has already been sent, a XMR-status is generated and the microcontroller has to repeat the complete frame again.

2.1.5 HDLC-Controller

The HDLC-controller performs the layer-2 functions of the D-channel protocol:

– Flag generation/detection
– Zero bit insertion/deletion
– CRC-generation/check (CCITT polynomial $X^{16} + X^{12} + X^6 + 1$)
– Abort generation
– Idle signal generation (‘1’)

HDLC-Frame Formatting

The HDLC-transmitter starts a HDLC-frame with a flag. It continues with the data of the XFIFO. The end of a frame is indicated by a closing flag preceeded by the 16-bit CRC-check sum or by an abort sequence.

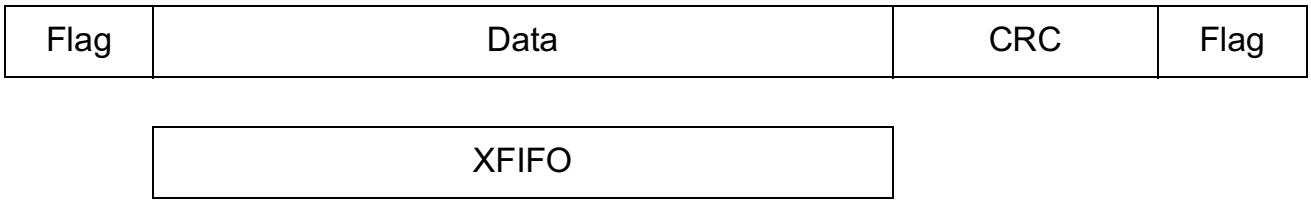


Figure 28
HDLC-Transmitter Format

The HDLC-receiver hunts for flags which are not followed by another flag or an abort sequence. It stores the information in the RFIFO until the end of the frame has been detected. The status of the received frame (CRC-status, end of frame condition etc.) is reported via a status byte which is stored in the RFIFO immediately following the last byte of a message.

The HDLC-receiver of the SmartLink will receive two frames correctly if they are separated by only one common flag (shared flag). It will also receive two frames correctly if they are separated by two flags (back-to-back frames).

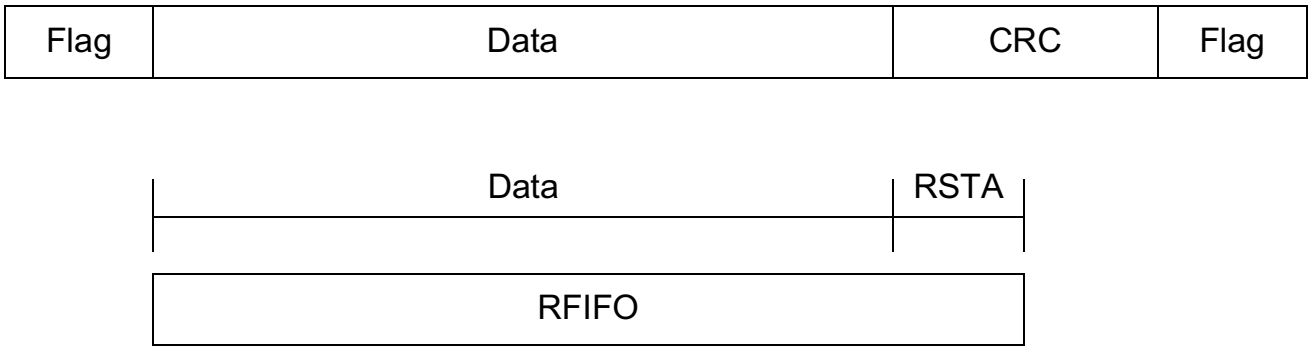


Figure 29
HDLC-Receiver Format

2.1.6 Terminal Specific Functions

2.1.6.1 LCD-Contrast Control

The Pulse Width Output/Ring provides a pulse width modulated signal which can be varied in 14 linear steps between OFF and ON. The repetition frequency is 8.5 kHz. The LCD-contrast control is enabled by setting the LCRI-bit to ‘0’.

The output of the PWM is filtered by a low pass filter and transformed to the required voltage range by an external transistor as shown in **figure 30**.

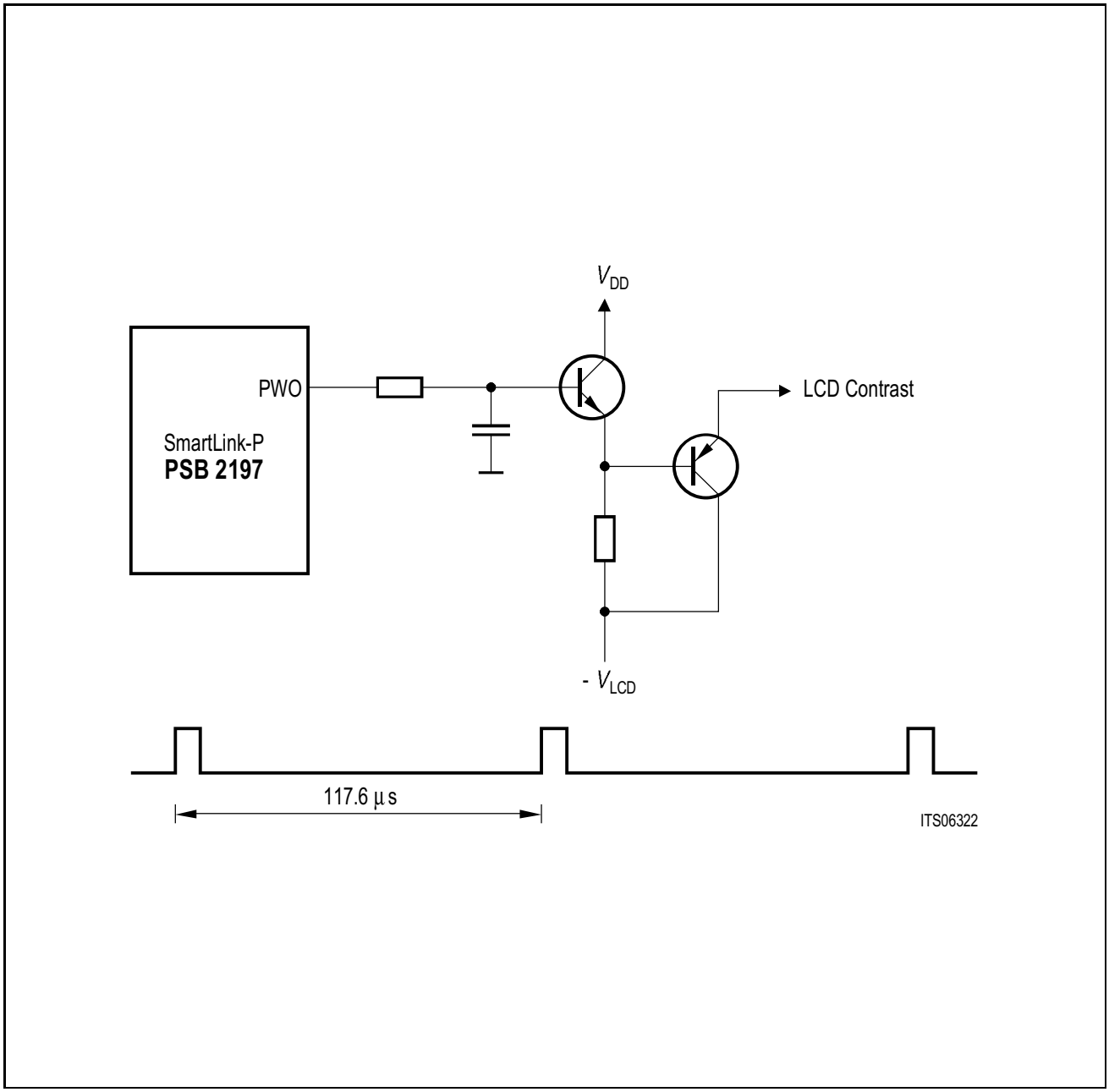


Figure 30
LCD-Contrast Control

2.1.6.2 Ring Tone Generation

The SmartLink-P can generate frequencies at the Pulse Width Output/Ring. The ring tone generator uses a 16 kHz-clock input and divides it by a programmable value of n = 1 to 63. The PWO/Ring output is tristate while PW5-0 are '000000'. The following list shows examples of frequencies:

Value	(PW5-0)	Frequency (Hz)
8	(001000)	2000
10	(001010)	1600
11	(001011)	1454
12	(001100)	1333
14	(001110)	1142
15	(001111)	1066
17	(010001)	941
19	(010011)	842
20	(010100)	800
21	(010101)	761
23	(010111)	695
27	(011011)	592
29	(011101)	551
33	(010001)	484
36	(100100)	444
41	(101001)	390
51	(110011)	313

Ring tones change or stop at the end of a half or full cycle. This includes switching to tristate.

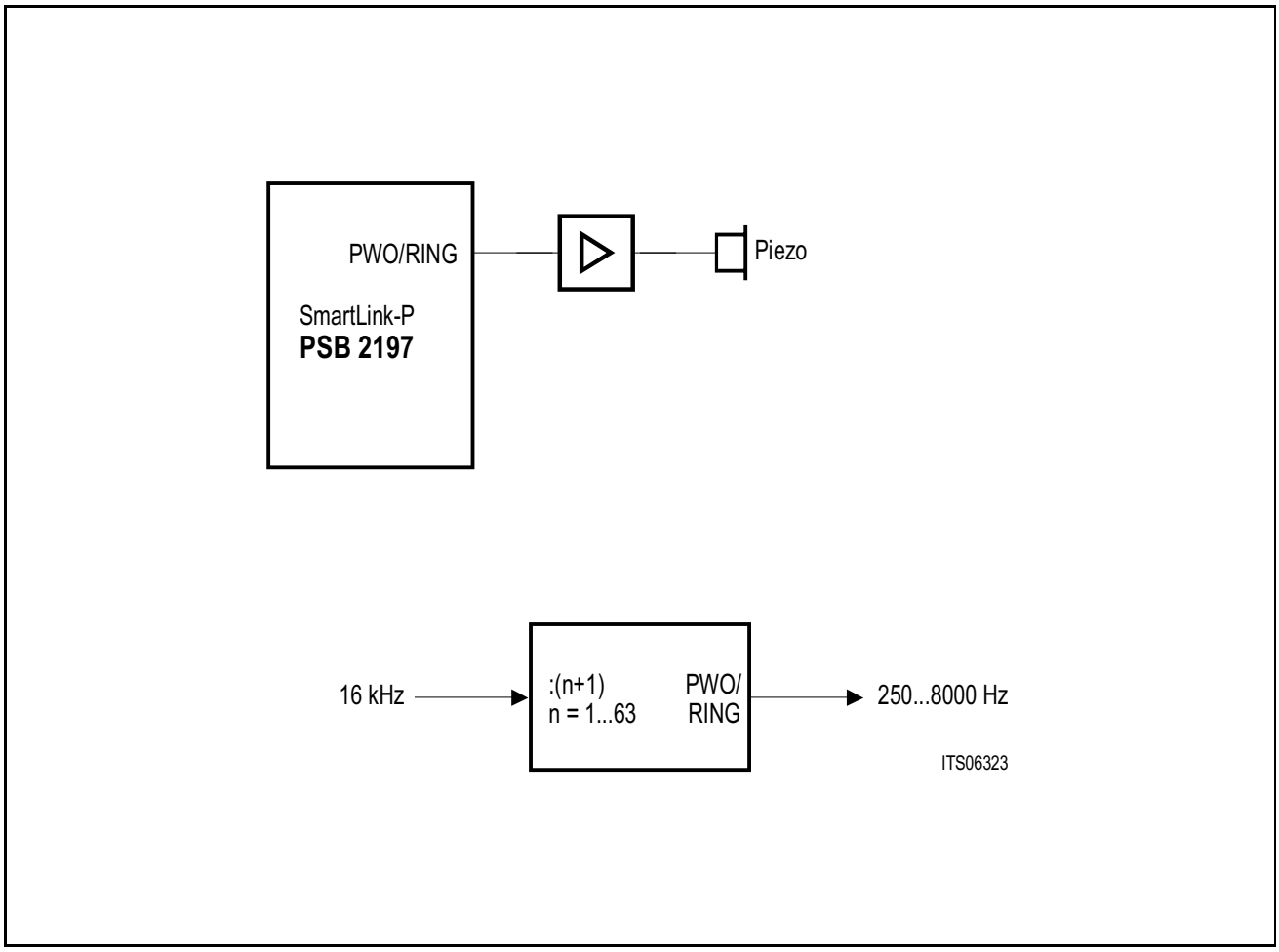


Figure 31
Ring Tone Generation

2.2 Terminal Repeater (TR) Mode

2.2.1 General Functions and Device Architecture (TR-Mode)

In TR-mode the following functions are provided:

- U_{pn}-interface transceiver, functionally fully compatible to both PEB 2095 IBC and PEB 2096 OCTAT-P, also features the terminal repeater mode
- IOM-2 interface for terminal application
- A microcontroller clock is not generated

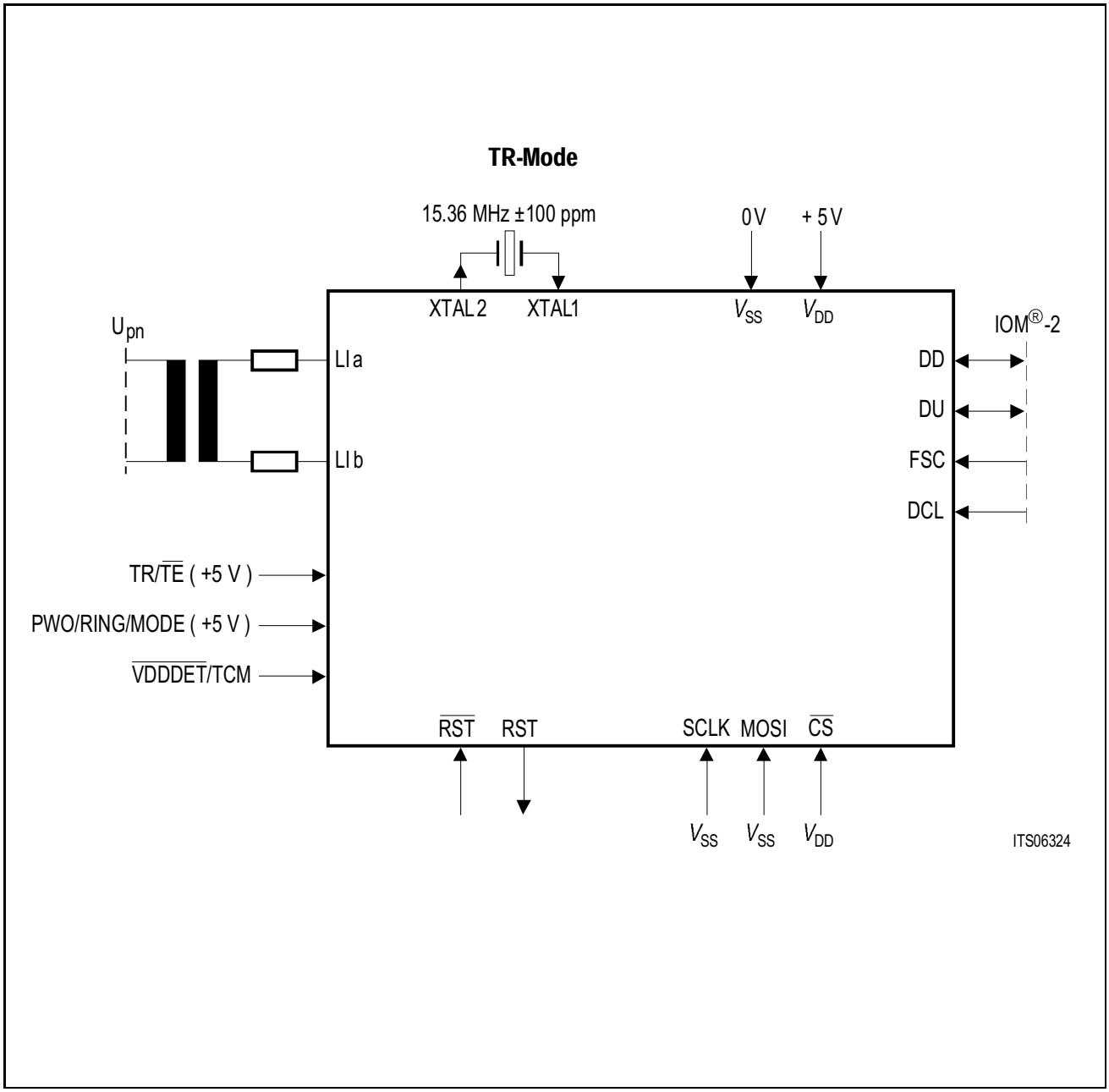


Figure 32
Device Architecture in TR-Mode

2.2.2 Clock Generation (TR-Mode)

In TR-mode, the oscillator is used to generate a 15.36-MHz clock signal. This signal is used by the DPLL to synchronize U_{pn}-frames to the received IOM-2 clocks (FSC, DCL). No other clocks are generated.

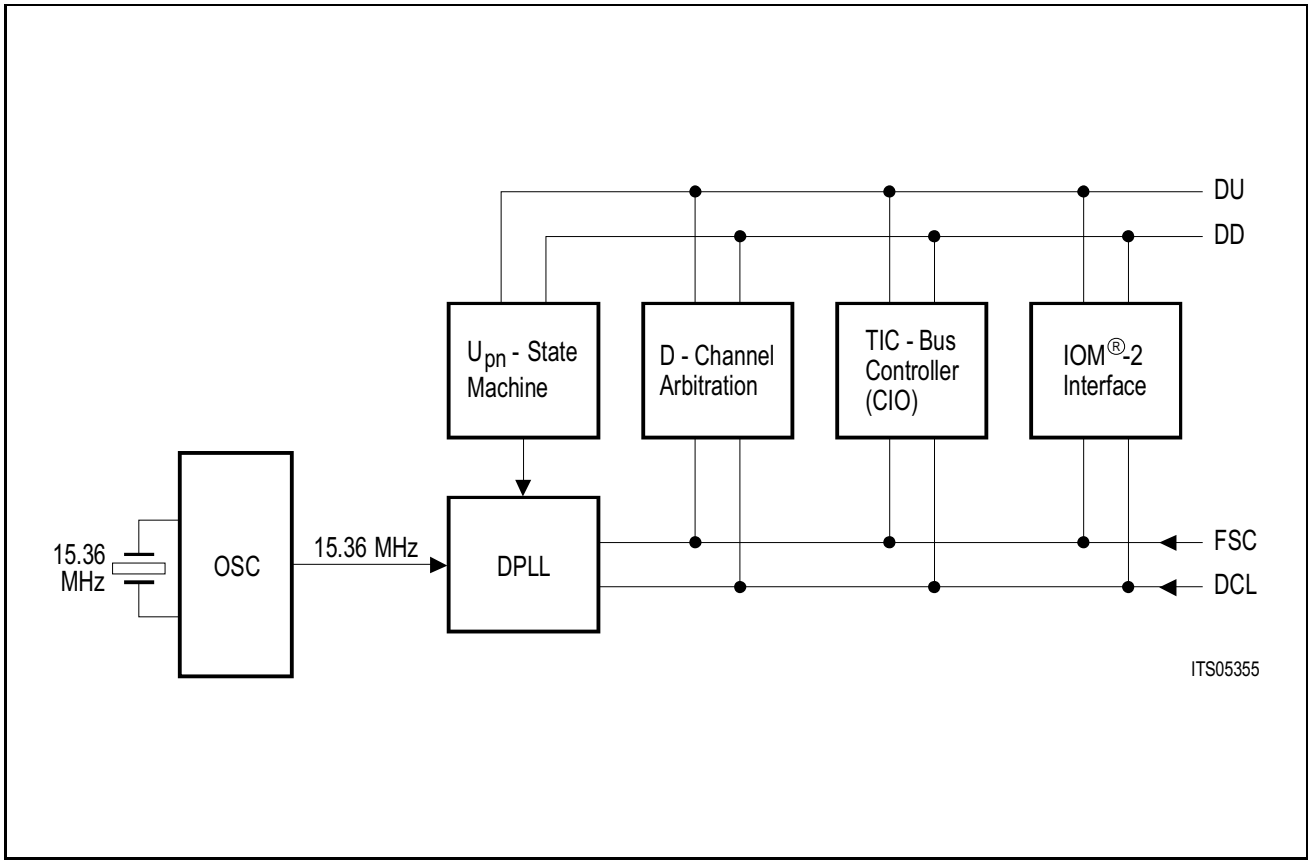


Figure 33
Clock Generation in TR-Mode

2.2.3 Interfaces (TR-Mode)

In TR-mode, two interfaces are active:

- IOM-2 interface: as a universal backplane for terminals
- U_{pn}-interface towards the two-wire slave subscriber line

The microcontroller interface remains active in TR-mode. As a result, the $\overline{CS}$-input has to be connected to V_{DD} and MOSI has to be connected to V_{SS} avoid accidental programming.

2.2.3.1 IOM®-2 Interface in TR-Mode

The SmartLink-P supports the IOM-2 terminal mode. The interface consists of four lines: FSC, DCL, DD and DU. FSC and DCL provide the clock inputs to synchronize the U_{pn}-transceiver to the IOM-2 interface. DU and DD are open drain outputs.

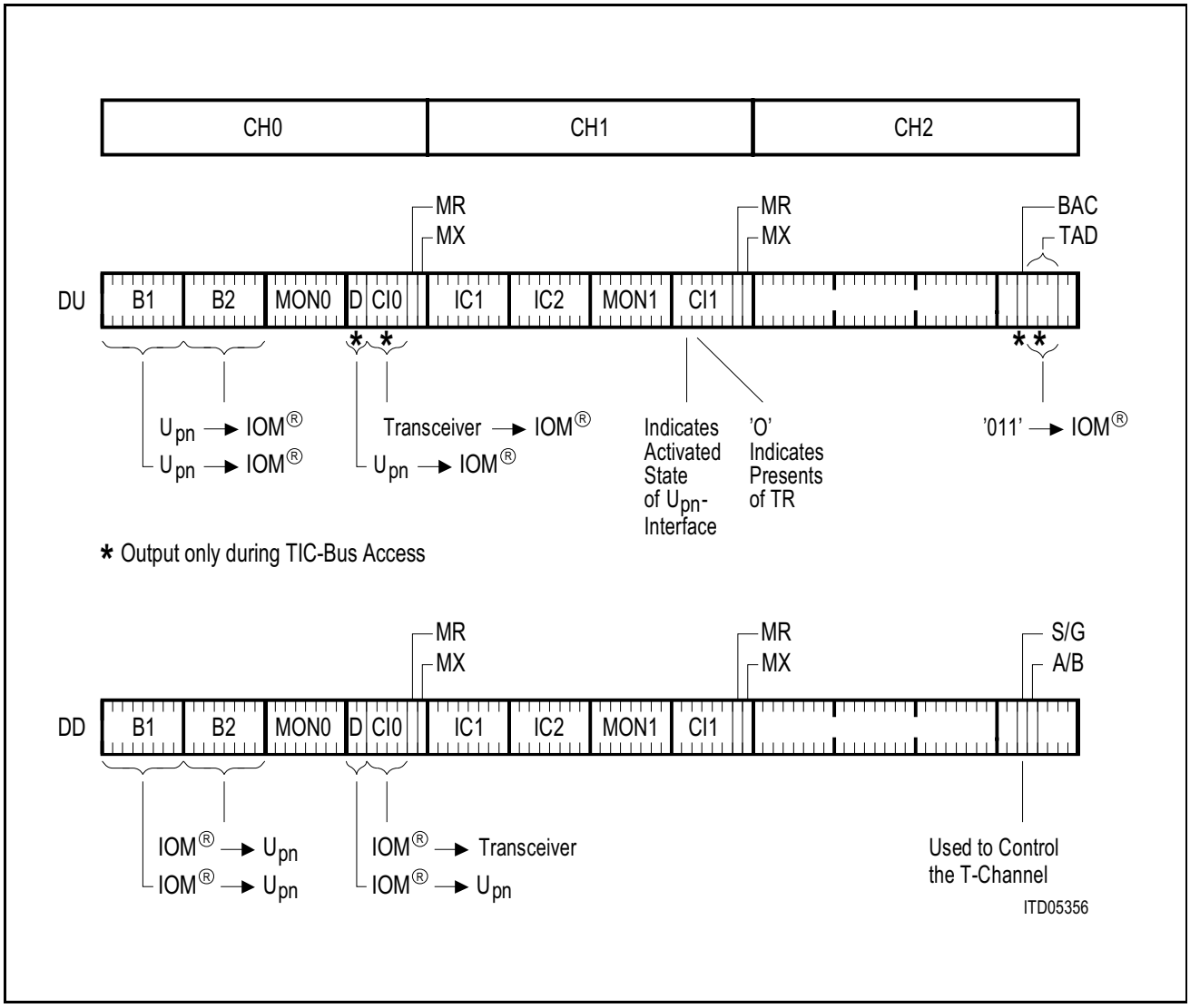


Figure 34
IOM®-2 Frame Structure in TR-Mode

The SmartLink-P transfers the B-channel information between the IOM-2 and the U_{pn}-interface during the activated state. During all other states, 'FF' is output. The C/I-channel 0 as well as the upstream D-bits are occupied by the TR-SmartLink after a TIC-bus access has been performed. The BAC- and TAD-bits are used for the TIC-bus access.

The SmartLink-P in TR-mode pulls bit 5 of the upstream command/indicate channel 1 to '0' after reset and remains '0' for identification of the TR-module by a terminal SmartLink-P or ISAC-P TE.

Bit 6 of the upstream C/I-channel 1 is also controlled by the SmartLink-P in TR-mode. It is set to '0' if the U_{pn}-interface is in the activated state. Otherwise, the bit remains '1'.

2.2.3.2 U_{pn}-Interface in TR-Mode

U_{pn}-Transceiver

The transmitter uses the received FSC-signal to start the generation of a U_{pn}-frame. If a short FSC-length ($1 \times$ DCL) is detected, the superframe counter is reset and the next U_{pn}-frame will transmit the CV in the M-bit. During normal length of the FSC-signal (64 DCL-clocks), the superframe counter is not changed.

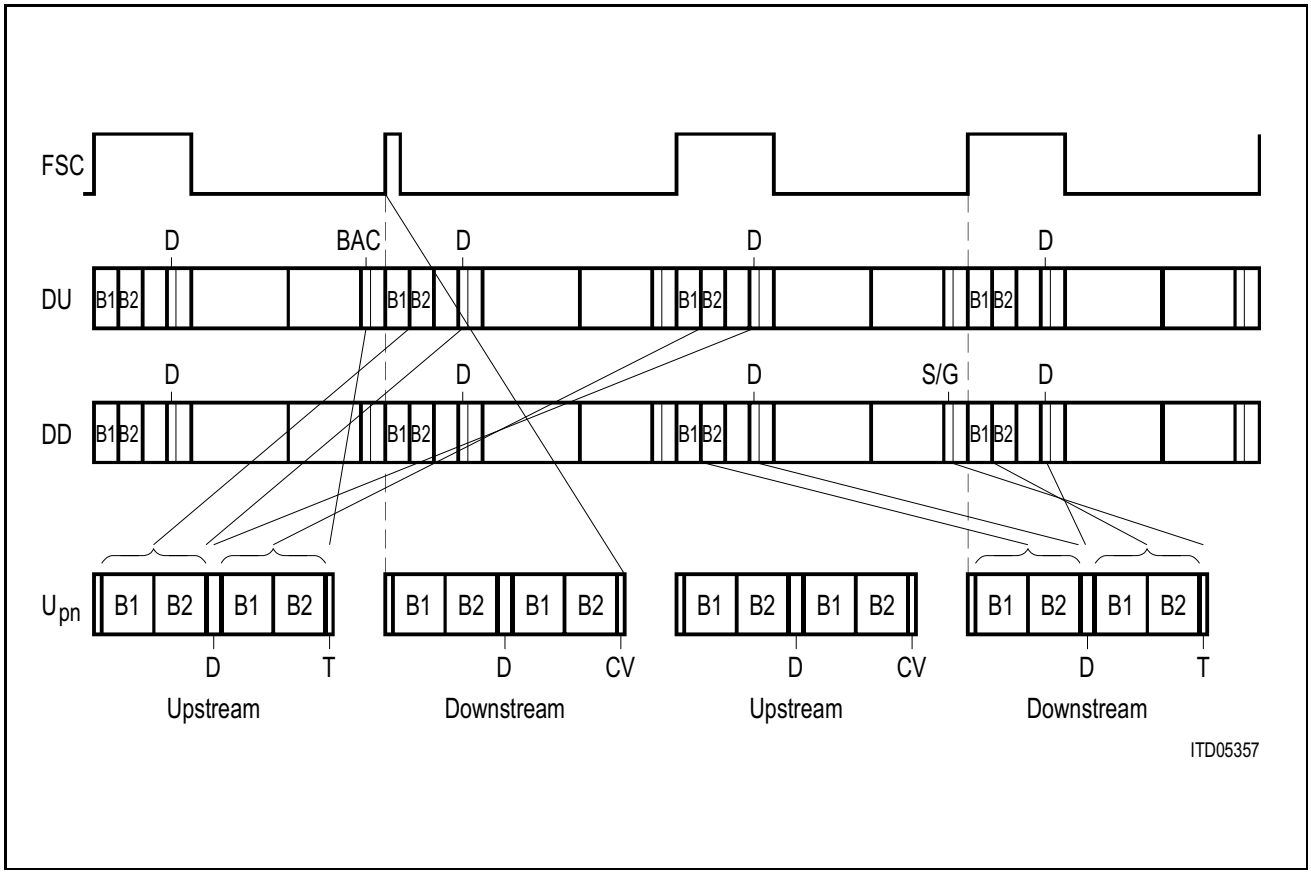


Figure 35
U_{pn}-Transceiver Timing

Control of the U_{pn}-Transceiver

An incorporated finite state machine controls the activation/deactivation procedures and communications with the layer-2 section via the IOM-Command/Indicate (C/I) channel 0.

In TR-mode, activation from the terminal side is started by a power-up sequence in case the FSC- and DCL-clocks are turned off. After that, a TIC-bus access is performed and activation is started by outputting the C/I-code 'AR'. After that, the U_{pn}-interface is activated and after completion of the procedure, the C/I-code 'AI' is output.

The length of the FSC-signal is monitored. The state-machine of the U_{pn}-transceiver is reset every time, a FSC-period of less than 96 bits is detected. It will generate a reset signal for the state machine which is active for 6 IOM-frames. As a result, 4 or 5 info 0 frames will be transmitted on U_{pn} a to force the TE-device in the level detect (resynchronization) state. This number of info 0 frames is still less than is required to detect Info 0 by the TE-device (2 ms, 8 info 0 frames). This procedure is necessary to avoid incorrect switching of internal B-channel buffers which corrupt the sequence of B-channel transfer between IOM and U_{pn}.

2.2.4 D-Channel-Arbitration in TR-Mode

The D-channel arbitration is done using the TIC-bus features and the T-channel of the U_{pn}-interface.

TIC-Bus Idle

If the TIC-bus is idle (BAC = '1', TAD = '111'), upstream D-channel data is transparently switched to the IOM-2 D-channel. No C/I0-code is transmitted by the TR-SmartLink.

D-Channel Request

A D-channel request is indicated by the terminal connected to the TR-SmartLink by setting the upstream T-channel to '1' (inverse of its IOM-2 BAC-bit). As a result, the TR-SmartLink tries to access the TIC-bus by outputting the TIC-bus address ('011'). After successful transmission of all three bits, the BAC-bit is set to '1' in the following IOM-2 frame and the TIC-bus is occupied. On the C/I-channel 0, the code 'AI' ('1100') is output.

D-Channel Release

After the terminal connected to the TR-SmartLink has completed its HDLC-frame, the upstream T-channel becomes '0' (inverse of its IOM-2 BAC-bit). This transition from T = '1' to T = '0' is delayed by the TR-SmartLink by two IOM-frames before the TIC-bus is released. This delay is necessary to assure that the D-channel contents of the U_{pn}-frame which included the T-channel is output completely.

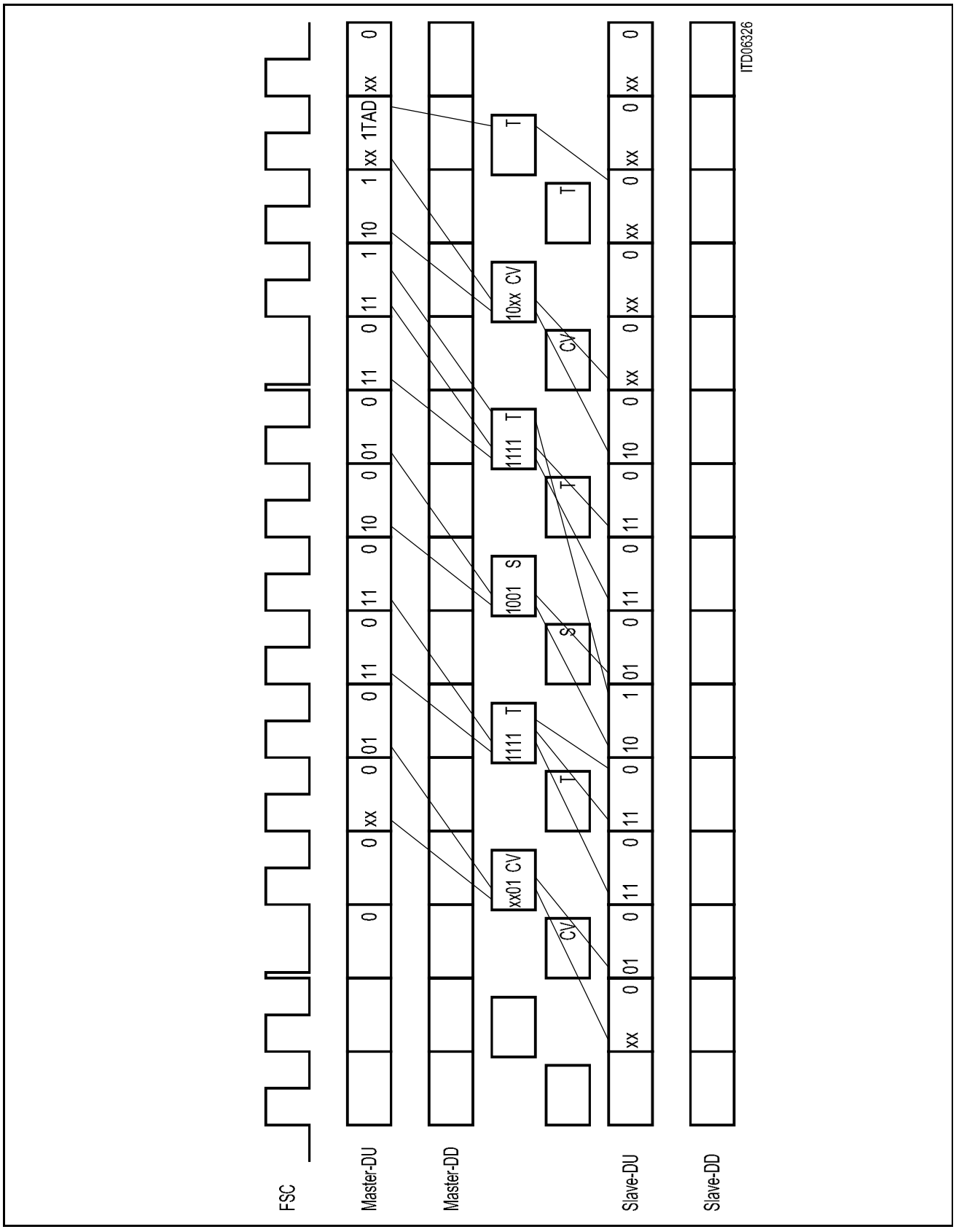


Figure 36
D-Channel Arbitration in TR-Mode

2.2.5 Reset

In TR-mode, the undervoltage detection is not active. To reset the SmartLink-P in TR-mode an external reset signal must be applied on the $\overline{RST}$ input. The reset will deactivate the U_{pn}-transceiver and it will abort any TIC-bus access currently in progress. The TIC-bus returns to idle.

While the reset signal is active, at least 40 clock pulses must be applied to XTAL1 and at least 4 DCL-pulses. More than 10 clock pulses on XTAL1 are required after reset becomes inactive. At least 6 IOM-frames are necessary after reset is released to put the U_{pn}-transceiver in its deactivated state from which an asynchronous awake is possible if a level is detected on the U_{pn}-interface pins.

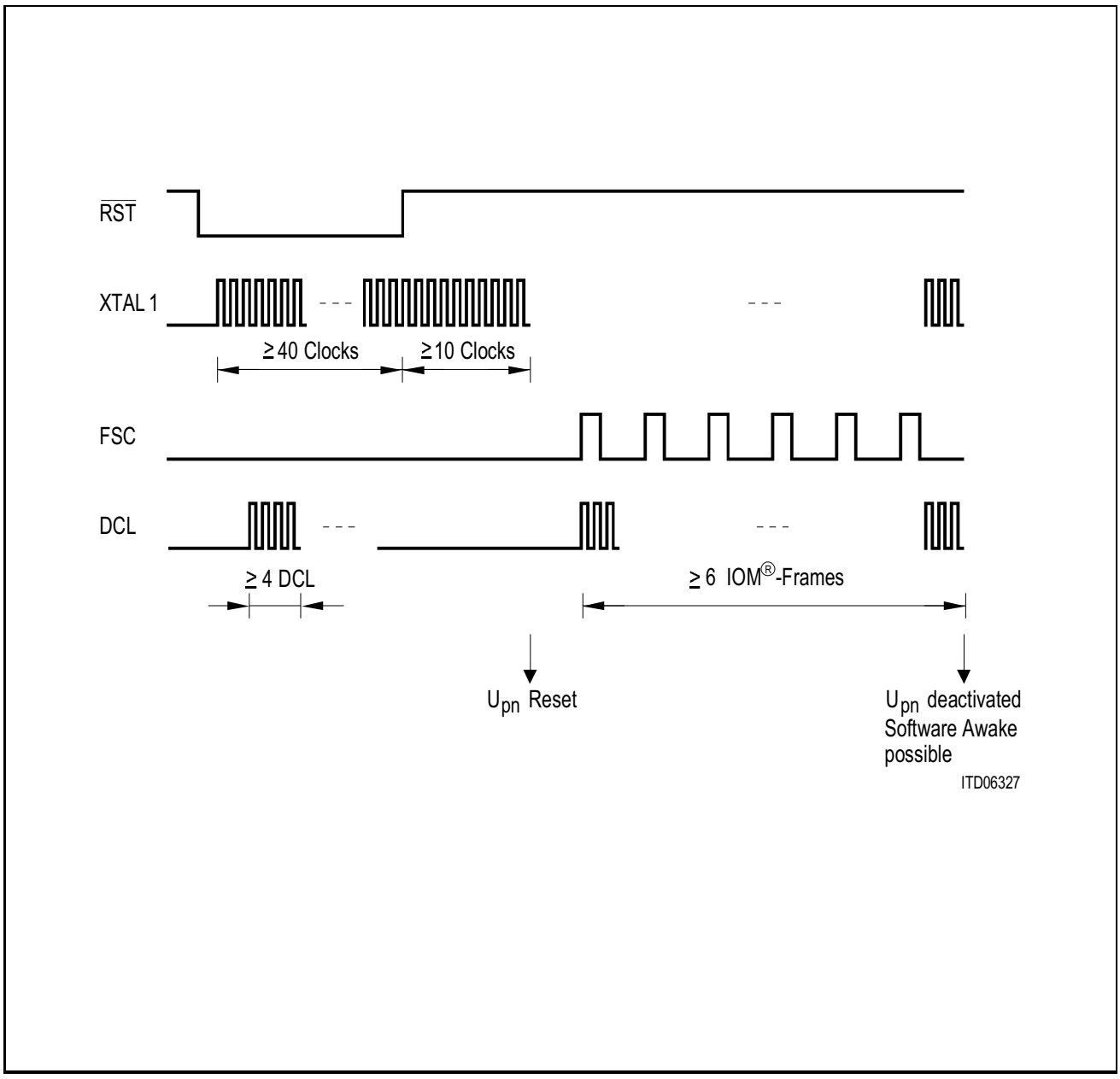


Figure 37

2.3 HDLC-Controller Mode

2.3.1 General Functions and Device Architecture (HDLC-Controller Mode)

Figure 38 depicts the detailed architecture of the PSB 2197 SmartLink-P in HDLC-controller mode:

- Serial control port
- HDLC-controller with 2 × 4 byte FIFOs per direction
- TIC-bus access control
- IOM-2 interface for terminal application

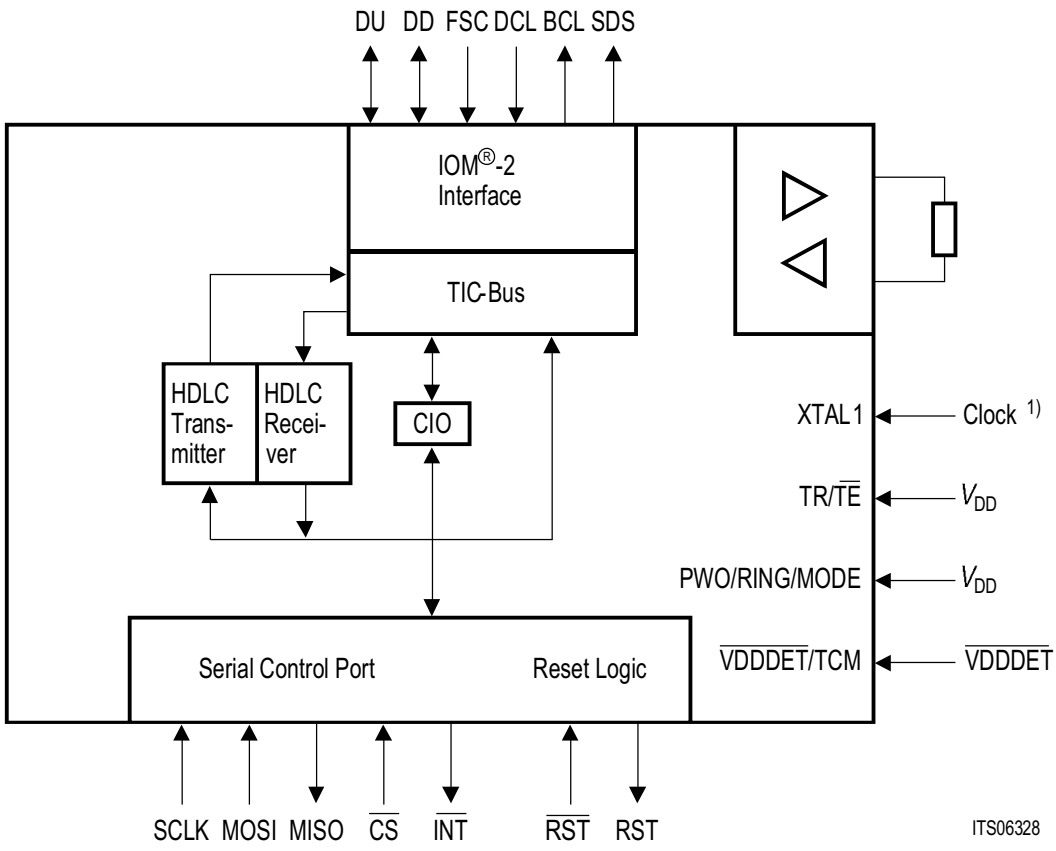


Figure 38
Device Architecture of the SmartLink-P in HDLC-Controller Mode

2.3.2 Clock Generation (HDLC-Controller Mode)

In HDLC-controller mode, the oscillator input is used to achieve the reset state of the U_{pn}-transceiver. All other functions which use the oscillator frequency in TE-mode (undervoltage detection, watchdog, microcontroller clock output, PWO/RING) are disabled. The IOM-2 clock signals (FSC, DCL) are used to synchronize the HDLC-data transfer and the access to the TIC-bus. A bit clock signal as well as a strobe signal for B1, B2 or IC1 may be generated.

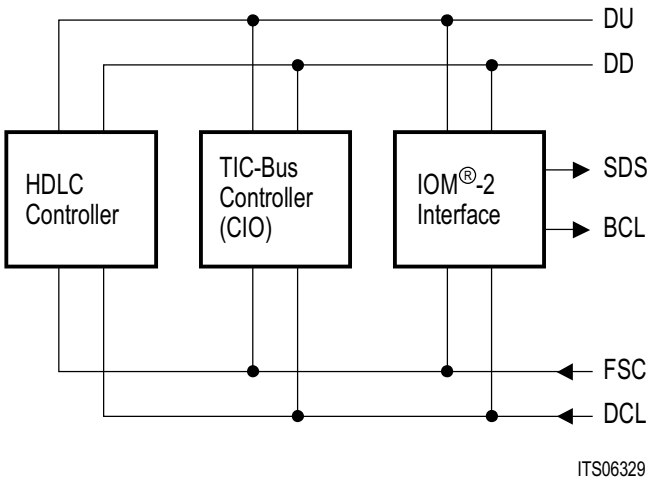


Figure 39
Clock Generation in HDLC-Controller Mode

2.3.3 Interfaces (HDLC-Controller Mode)

The PSB 2197 SmartLink-P serves two interfaces in HDLC-controller mode:

- Serial microcontroller interface for higher layer functions
- IOM-2 interface: between layer-1 and layer-2 and as a universal backplane for terminals
- Bit clock and strobe signal generation

2.3.3.1 Microcontroller Interface

The SmartLink-P provides a serial microcontroller interface which is compatible to the SPI-interface of Motorola or Siemens C510x microcontrollers.

Its function is identical to the TE-mode.

2.3.3.2 IOM®-2 Interface in HDLC-Controller Mode

The SmartLink-P supports the IOM-2 terminal mode. The interface consists of four lines: FSC, DCL, DD and DU. FSC and DCL provide the clock inputs to synchronize the data transfer over the IOM-2 interface. DU and DD are open drain outputs.

A bit clock and strobe signal may be generated locally.

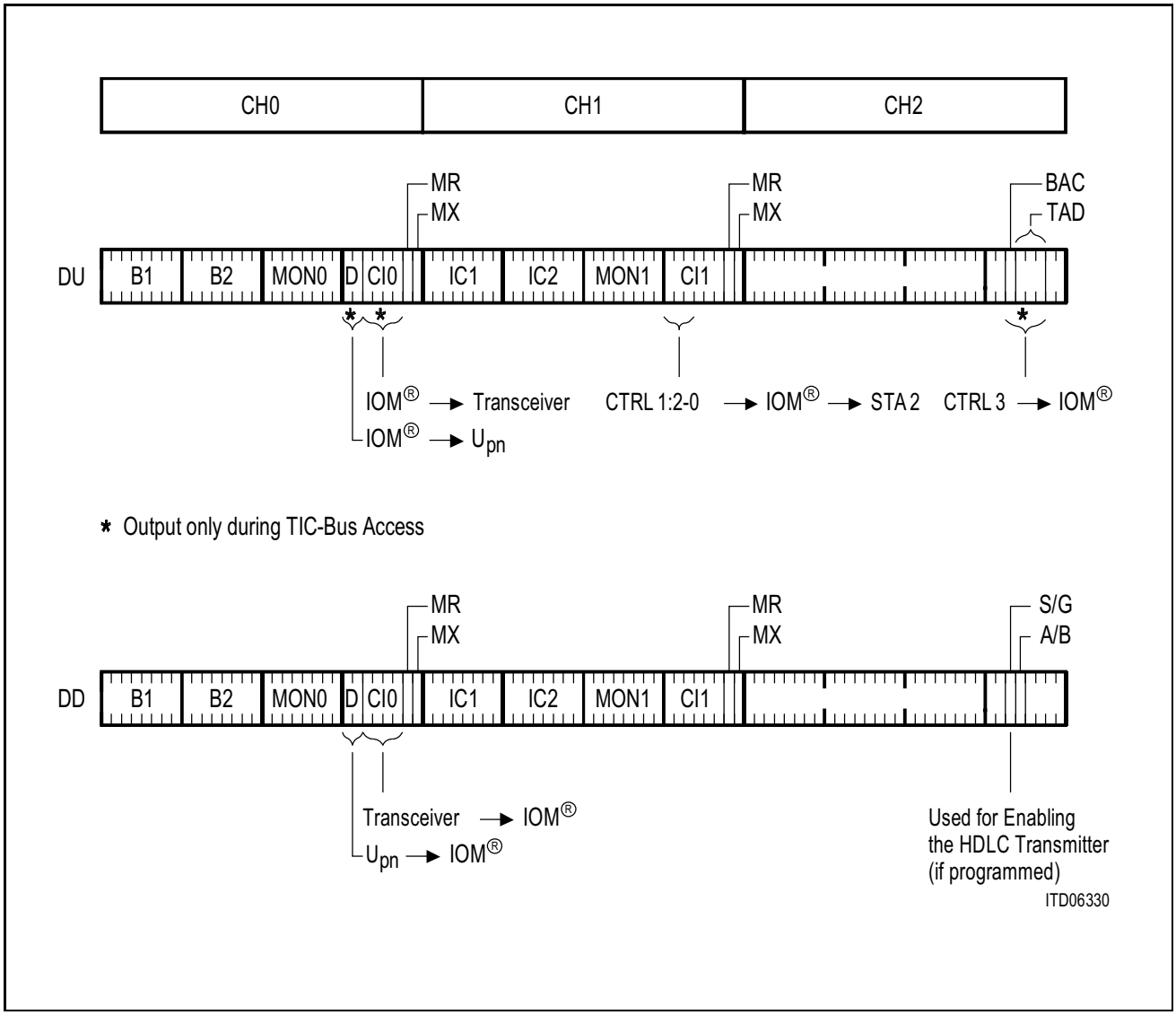


Figure 40
IOM®-2 Frame Structure in HDLC-Controller Mode

The C/I-channel 0 as well as the upstream D-bits are occupied by the HDLC-controller mode SmartLink after a TIC-bus access has been performed. The BAC- and TAD-bits are used for the TIC-bus access.

The SmartLink-P in HDLC-controller mode outputs the value of CTRL1:2-0 as CI1 bits 7 to 5. After reset, they remain ‘1’.

All other time-slots are not influenced by the SmartLink-P in HDLC-controller mode.

2.3.4 D-Channel-Arbitration in HDLC-Controller Mode

The D-channel arbitration is identical to the one in TE-mode.

2.3.5 HDLC-Controller

The HDLC-controller functions are identical to the ones in TE-mode.

2.3.6 Reset

The HDLC-controller mode is reset by applying a reset pulse to the RST-input.

To bring the U_{pn}-transceiver to a low power state, the following requirements must be fulfilled: While reset is active, at least 40 clock pulses must be applied to XTAL1. After reset is released, another 10 clock pulses are required. The U_{pn}-transceiver enters its low power deactivated state after 6 IOM-frames which are generated after the 50 clock pulses on XTAL1 have elapsed.

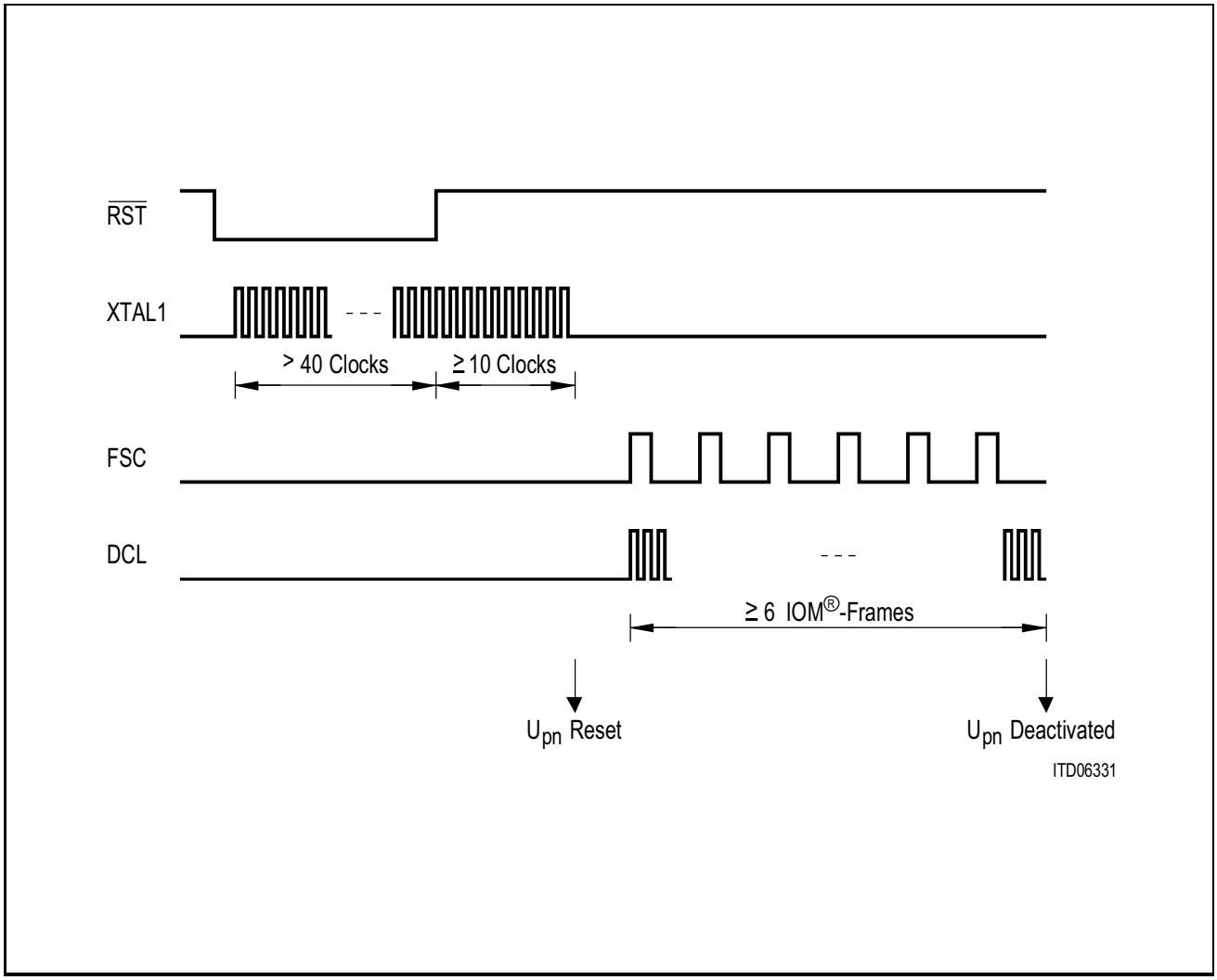


Figure 41
Reset

3 Operational Description

3.1 TE-Mode

3.1.1 Interrupt Structure and Logic

The SmartLink-P provides one interrupt output which is used to indicate a change in the receiver or transmitter status or a change in the CI0-code. The microcontroller has to read the first status byte (STA1). The first status byte indicates changes of the receiver/transmitter section. CI0-code changes are indicated by the CIC-bit. In case of a CI0-change, the microcontroller has to evaluate the second status byte (STA2). It contains the new CI0-code value. Reading the STA1-status byte clears the interrupt request and the RPF-, RME-, XFS-, RFO-bits. The CIC-status bit and the interrupt generation by that bit is cleared by reading STA2.

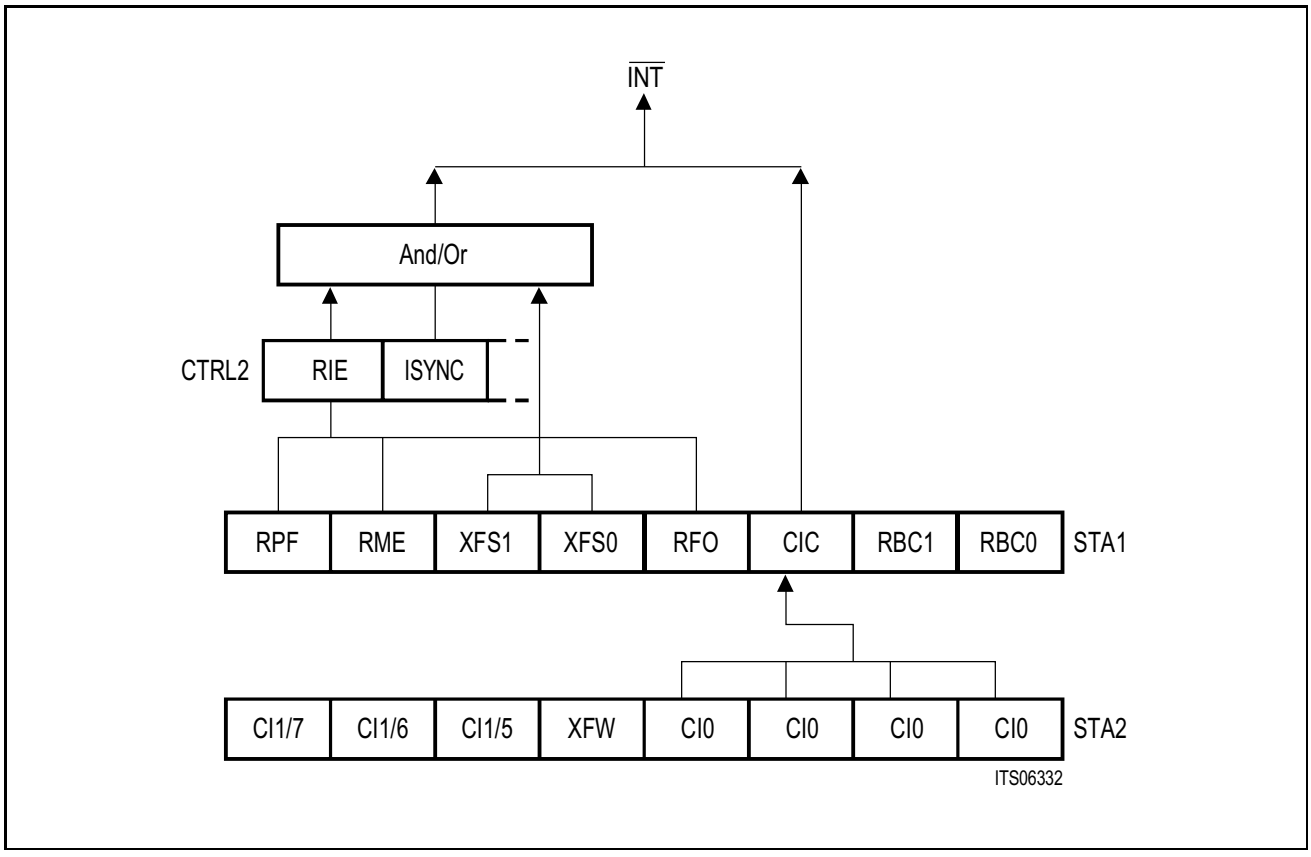


Figure 42
SmartLink-P Interrupt Structure

The transmitter and C/I-change interrupts are permanently enabled. The generation of receiver interrupts is enabled by the RIE-bit. After reset, this bit is cleared and receiver interrupts are disabled.

Changes in the received CI1-bits as well as a change in the XFW-bit will never generate an interrupt.

3.1.2 Control of the U_{pn}-Transceiver

3.1.2.1 Power-Down of the IOM®-2 Interface

In order to reduce power consumption in the non-operational status the IOM-2 interface is brought into power down while the U_{pn}-transceiver is in the deactivated state. The clocks are stopped at bit position 30 (starting with 1). FSC remains high, DCL remains at low voltage level, the data lines remaining pulled up by the external pull up resistors. For the exact procedures please refer to the IOM-2 Reference Guide Edition 3.91.

Since the length of the FSC-signal is reduced every eight frames, the oscillator stops only during the regular length of a FSC-signal.

BCL and SDS if enabled remain ‘0’ during power-down.

During power-down state (C/I = ‘1111’), only the IOM-clock signals are turned off. The oscillator, the U_{pn}-awake detector is active as well as the microcontroller clock, pulse width modulator clock and watchdog counter.

The power-down state is left when an asynchronous awake signal has been detected. The IOM-clocks are started. After the asynchronous awake signal is stopped, one device on IOM-2 must output CI0-codes different from ‘DI’ (Deactivation Indication, ‘1111’) to keep the IOM-2 interface running.

The asynchronous awake may be generated by any device by pulling the DU-line to ‘0’. The SmartLink in TE-and HDLC-controller mode can force DU to ‘0’ by setting the SPU-bit in CTRL4.

3.1.2.2 Activation/Deactivation of the U_{pn}-Interface

The U_{pn}-transceiver functions are controlled by commands issued in the CTRL4-register. These commands are transmitted over the C/I-channel 0 and trigger certain procedures such as activation/deactivation and switching of test loops. Indications from layer-1 are obtained by evaluating the second status byte (STA2) after a CIC-status is indicated (STA1).

3.1.2.3 Layer-1 Command/Indication Codes in TE-Mode

Command (Upstream)	Abbr.	Code	Remarks
Timing	TIM	0000	Layer-2 device requires clocks to be activated
Reset	RES	0001	Software reset
Send Single Pulses	SSP	0010	Ones (AMI) pulses transmitted at 4 kHz
Send Continuous Pulses	SCP	0011	Ones (AMI) pulses transmitted continuously
Activate Request	AR	1000	
Activate Request Loop 3	ARL	1001	Local analog loop
Deactivation Indication	DI	1111	

Indication (Downstream)	Abbr.	Code	Remarks
Deactivation Request	DR	0000	
Power-Up	PU	0111	
Test Mode Acknowledge	TMA	0010	Acknowledge for both SSP and SCP
Resynchronization	RSY	0100	Receiver not synchronous
Activation Request	AR	1000	Receiver synchronized
Activation Request Loop 3	ARL	1001	Local loop synchronized
Activation Request Loop 2	ARL2	1010	Remote loop synchronized
Activation Indication	AI	1100	
Activation Indication Loop 3	AIL	1101	Local loop activated
Activation Indication Loop 2	AIL2	1110	Remote loop activated
Deactivation Confirmation	DC	1111	Line and IOM-interface are powered down

3.1.2.4 State Diagrams

Activation/Deactivation

The internal finite state machine of the PSB 2197 SmartLink-P controls the activation/deactivation procedures. Such actions can be initiated by signals on the U_{pn}-transmission line (INFO's) or by control (C/I) codes sent over the C/I-channel 0 of the IOM-interface.

The exchange of control information in the C/I-channel is state oriented. This means that a code in the C/I-channel is repeated in every IOM-frame until a change is necessary. A new code must be recognized in two consecutive IOM-frames to be considered valid (double last look criterion).

The activation/deactivation procedures implemented by the PSB 2197 SmartLink-P agree with the U_{pn}-interface as it is implemented by the PSB 2196 ISAC-P TE.

In the state diagrams a notation is employed which explicitly specifies the inputs and outputs on the U_{pn}-interface and in the C/I-channel 0.

3.1.2.5 TE-Mode State Description

Reset, Pending Deactivation

State after reset or deactivation from the U_{pn}-interface by info 0. Note that no activation from the terminal side is possible starting from this state. A 'DI'-command has to be issued to enter the state deactivated.

Deactivated

The U_{pn}-interface is deactivated and the IOM-2 interface is or will be deactivated. Activation is possible from the U_{pn}-interface and from the IOM-2 interface.

Power-Up

The U_{pn}-interface is deactivated and the IOM-2 interface is activated, i.e. the clocks are running.

Pending Activation

Upon the command Activation Request (AR) the PSB 2197 SmartLink-P transmits the 2-kHz info 1w towards the network, waiting for info 2.

Level Detect, Resynchronization

During the first period of receiving info 2 or under severe disturbances on the line the U_{pn}-receiver recognizes the receipt of a signal but is not (yet) synchronized.

Synchronized

The U_{pn}-receiver is synchronized and detects info 2. It continues the activation procedure by transmission of info 1.

Activated

The U_{pn}-receiver is synchronized and detects info 4. It concludes the activation procedure by transmission of info 3. All user channels are now conveyed transparently.

Analog Loop 3 Pending

Upon the C/I-command Activation Request Loop (ARL) the PSB 2197 SmartLink-P loops back the transmitter to the receiver and activates by transmission of info 1. The receiver is not yet synchronized.

Analog Loop 3 Synchronized

After synchronization the transmitter continues by transmitting info 3.

Analog Loop 3 Activated

After recognition of the looped back info 3 the channels are looped back transparently.

Test Mode Acknowledge

After entering test mode initiated by SCP-, SSP-commands.

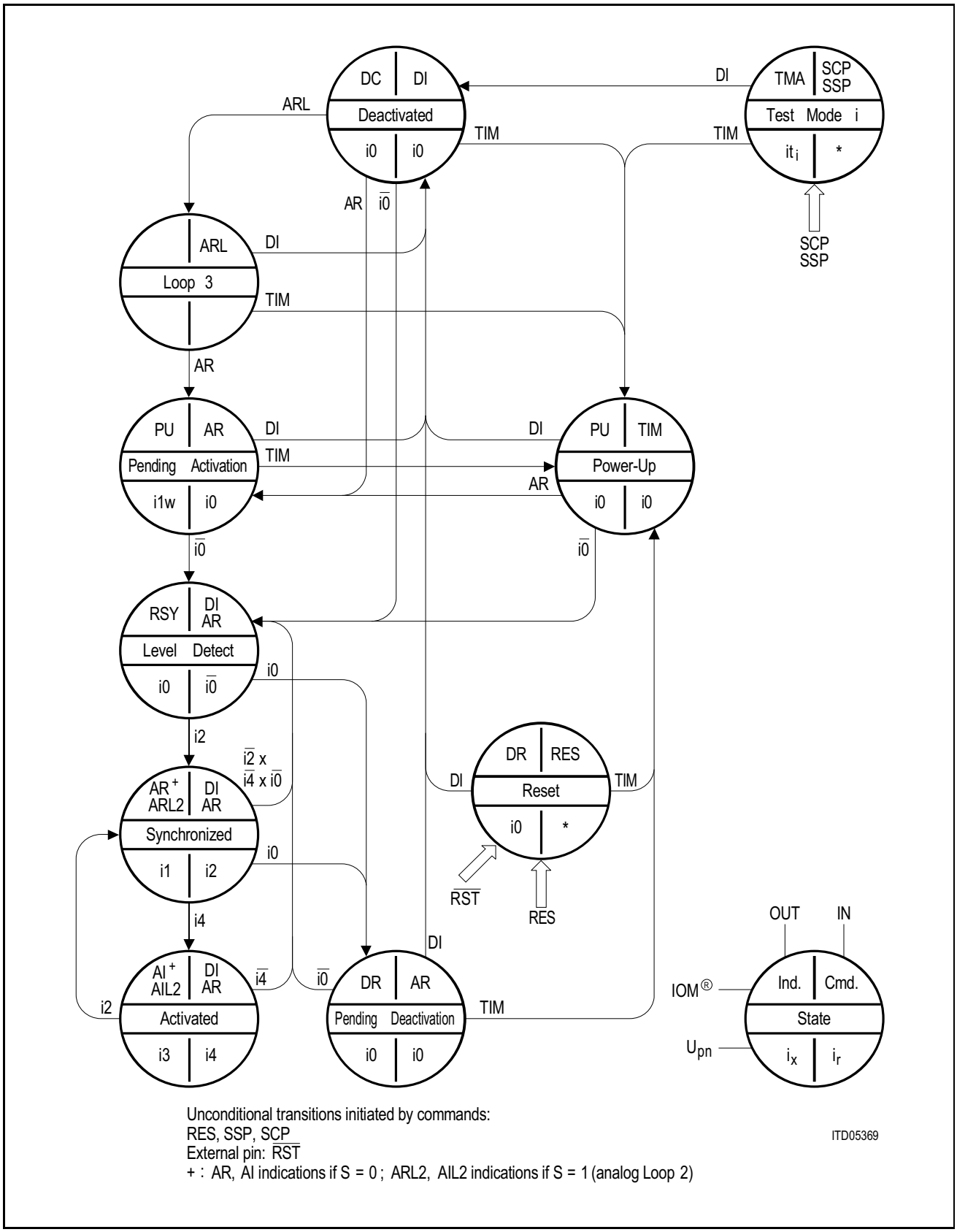


Figure 43
State Diagram TE-Mode

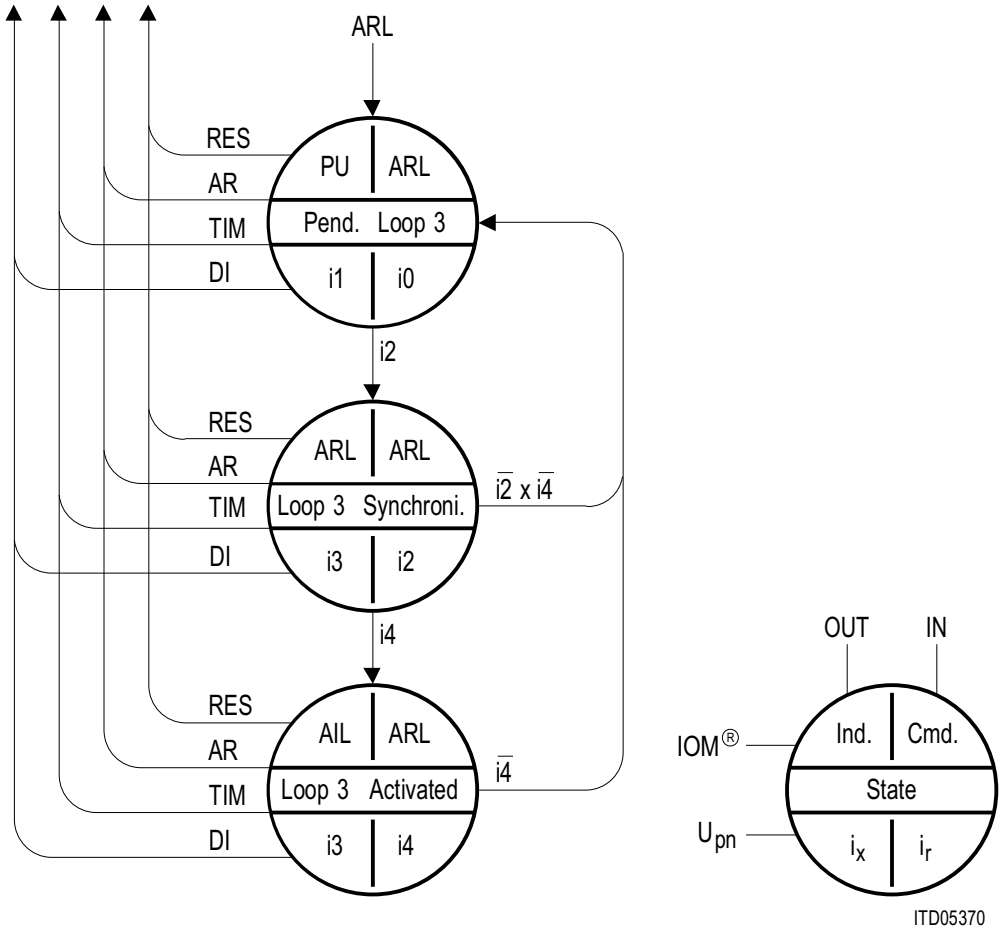


Figure 44
State Diagram TE-Mode (Test Loop 3)

3.1.2.6 Example of the Activation/Deactivation

Figure 45 shows the activation/deactivation procedure between the line card (Octat-P) and the terminal (SmartLink-P).

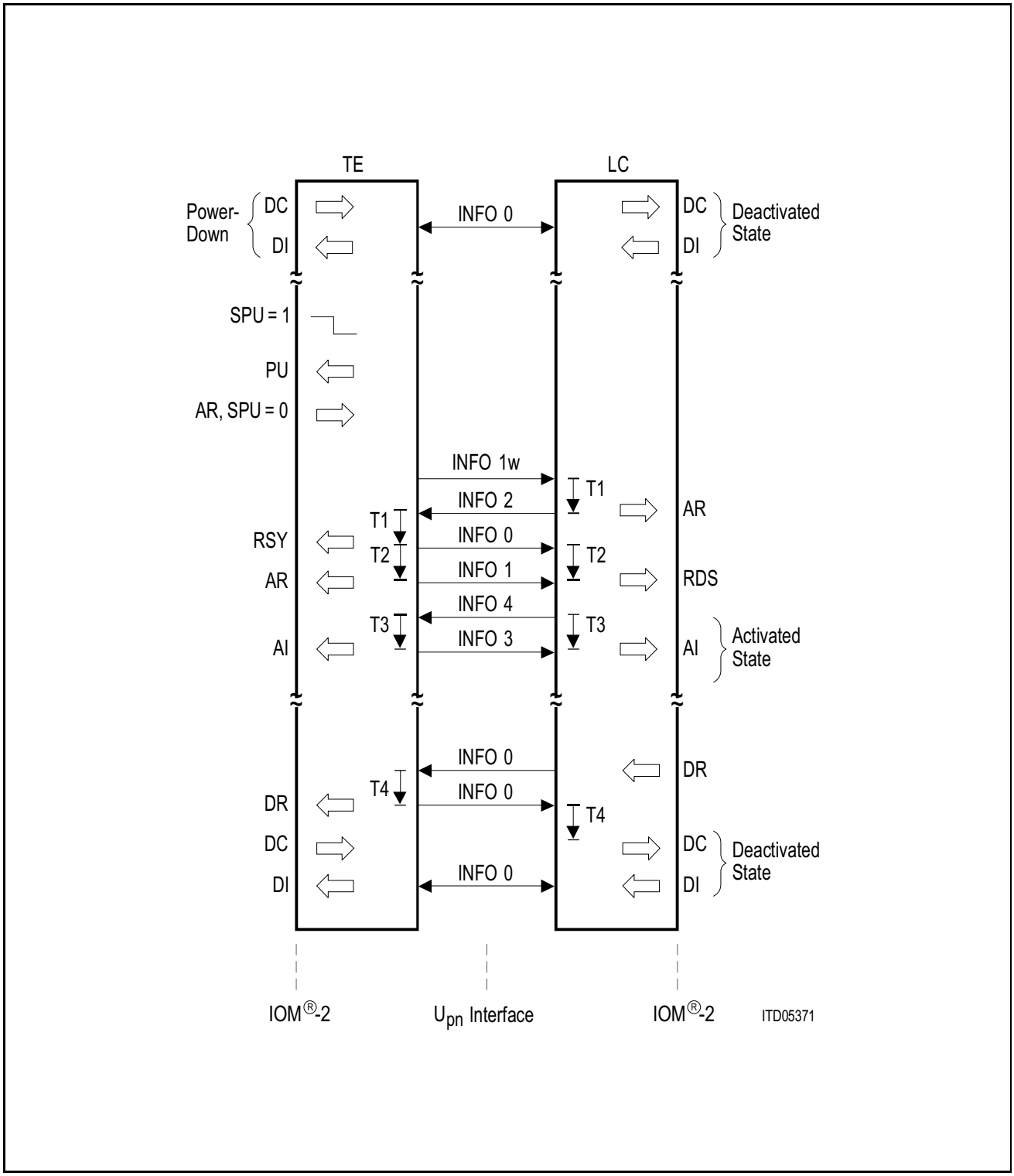


Figure 45
Activation/Deactivation (LC, TE)

3.1.3 Operation of the Serial Control Interface

A state machine controls the operation of the serial control port. It performs the necessary read and write operations to the internal registers.

Begin of Transmission

The begin of a transmission is indicated by pulling $\overline{CS}$ low. This will force the MISO-output to drive the current value of the shift register output. At the same time, the execution of HDLC-controller commands is disabled.

The first falling edge will force the state machine to load the current value of STA1 into the shift register and output the MSB. The following clocks shift the contents of STA1 over the MISO-line. At the same time, the MOSI-line receives the value of CTRL1. Its value is stored in the CTRL1-register with the rising edge of the last clock period.

The state machine will transfer the contents of STA2 into the shift register at the next falling edge on the clock line and outputs the MSB of the shift register. The next clock pulses transfer the STA2-value while CLTR2 is received. The rising edge of the eighth clock period is used to transfer the contents of the shift register into CTRL2-register. The command bits are disabled until the end of the transfer.

In transmit direction (SmartLink-P $\rightarrow$ µP), the contents of RFIFO-data will follow if a receive status condition was reported and receiver command has not been issued. Similar to register accesses, this occurs with the first falling edge of the clock signal.

In receive direction (µP $\rightarrow$ SmartLink-P), the operation of the state machine depends on the value of XBC1, 0 and HXC1, 0 bits.

If HXC1, 0 indicates a XTF or XTF $\times$ XME-command, the number of bytes indicated in XBC1, 0 are received and transferred into the XFIFO with the rising edge of every eighth clock signal.

If HXC1, 0 indicates no command (‘00’) and XBC1, 0 indicates ‘01’, the following two bytes are stored in CTRL3 and CTRL4 with the rising edge of every eighth clock signal. RFIFO-data is not output if CTRL2 indicates that CTRL3 and CTRL4 will follow.

All further information will be ignored.

End of Transfer

At the end of the transfer which is determined by the $\overline{CS}$-line to become high, the commands (XTF, XTF $\times$ XME, XRES, RMC, RMD, RRES) are enabled again.

Error Detection

The state machine monitors the number of bits transferred. Only if eight bits have been transmitted, the contents of the shift register is transferred into the proper register. No special error indication is provided.

In order to avoid locking of the HDLC-operation by a spurious clock pulse on the serial control interface, two additional status bits are added.

RFO (Receive Frame Overflow) indicates that the start of a frame could not be stored in the RFIFO. This indication is helpful if the value of the STA1-byte has been changed so that the RPF- or RME-status bit was not transferred correctly. The microcontroller has to acknowledge the RFIFO by RMC-commands until all frames which were buffered in the RFIFO have been read. XFW (Transmit FIFO Write Enable) informs that the XFIFO is free and data can be entered. In case a XPR-status bit is not transferred correctly over the serial control interface, the microcontroller may poll the XFW-bit after a certain period of time to see if the XFIFO is accessible.

Timing between Bytes

The bytes can follow immediately or with gaps between the bytes. There is no maximum pause specified. The only requirement is that the $\overline{CS}$-line remains active during the gap.

Minimum Pause between Accesses

A minimum time of 10 DCL clocks must elapse between two accesses to the serial control interface ($\overline{CS}$ becoming low) to assure that a previously entered command is executed correctly.

3.1.4 Control of the HDLC-Data Transfer

The control of the HDLC-data transfer is optimized for full duplex operation via the serial control interface. A standard interrupt response takes up to six bytes to read/write the HDLC FIFOs.

3.1.4.1 HDLC-Transmitter

The HDLC-transmitter consists of a 2×4 byte FIFO. One half is connected with the transmit shift register while the other half is accessible via the microcontroller interface. Two status bits are controlled by the HDLC-transmitter to indicate a new status. The HDLC-transmitter is controlled by two bits which act as command. The corresponding bits of the CTRL2-register start the command. After the command has been executed, these bits are reseted automatically.

One command is used to indicate that the contents of the XFIFO is part of a frame and has to be transmitted (XTF). Another command (XTF $\times$ XME) indicates that the final part of a message has been entered into the XFIFO and has to be transmitted. In this case, the CRC-bytes as well as the closing flag is appended to the last byte from the XFIFO. The last command (XRES) resets the HDLC-transmitter, aborts a HDLC-frame currently in transmission and generates an XPR-status after the command has been completed. A new frame immediately entered after the XPR-status bit was set is delayed until the abort sequence has been completed.

Three state changes are indicated by the transmit FIFO-status bits. XPR indicates that the FIFO is able to load up to four new bytes to begin a message or to continue the frame. XMR indicates that the current frame has been aborted via the S/G-bit after the first FIFO-contents. The data of the frame has to be reentered. A XPR-status is generated immediately after XMR has been read to indicate that the FIFO is able to load new data. XDU indicates that the contents of the FIFO has been transmitted and no end-of-frame indication was issued. The transmitted frame has been aborted by a sequence of seven ‘1’.

XFS1	XFS0	Status	State	Action
0	0		No status change	Non or enter begin of message
0	1	XPR	Transmit Pool Ready	Enter up to four bytes
1	0	XMR	Transmit Message Repeat	Retransmit the message
1	1	XDU	Transmit Data Underrun	Frame has been aborted

The HDLC-transmitter and the transmit buffer are controlled by two bits of the second control byte (CTRL2).

HXC1	HXC0	Command	State
0	0		No command
0	1	XTF	Transmit Transparent Frame
1	0	XTF × XME	Transmit Transparent Frame and Transmit Message End
1	1	XRES	Transmitter Reset

3.1.4.2 HDLC-Receiver

The HDLC-receive FIFO contains 2×4 bytes. One half of the RFIFO (top half) is connected to the receiver shift register while the second half (CPU half) is accessible from the microcontroller. Data is stored into the top half until the second half is empty. If all four bytes contain valid data or the final part of a frame is stored in the CPU half, a status bit is set. The RPF-status bit indicates that all four bytes contain valid data which do not contain the last part of a message. The RME-interrupt indicates that the final part of a message is available from the RFIFO. In this case, the value of the RBC-bits have to be evaluated to determine the number of valid bytes in the RFIFO. At the end of the RFIFO-data transfer, a RMC-command has to be issued via the CTRL2-register. This command acknowledges the previous RPF- or RME-status and empties the RFIFO so that the next part of the frame or the next frame may be transferred from the top half to the CPU half. The RMC-command may also be sent if none of the RFIFO-data has been read.

The HDLC-receiver is controlled by two bits. Their combination indicates to reset the receiver, to acknowledge the RFIFO-contents, to ignore the remaining part of a frame. The later command can be used to suppress further reception of a frame after the address field has been received and it indicates a different destination.

Appr.	State	Action
RPF	Receive Pool Full	Four valid bytes are in the RFIFO. The RMC, RMD or RRES-command free's the RFIFO.
RME	Receive Message End	Up to four bytes are in the RFIFO. RBC1, 0 determine the number of valid bytes. The RMC, RMD or RRES-command free's the RFIFO.

HRC1	HRC0	Command	
0	0		No command
0	1	RMC	Acknowledges a previous RPF- or RME-status. The CPU RFIFO half can be used to store the next frame or the next part of a frame.
1	0	RMD	The remaining part of a message is not forwarded and the receiver FIFO is cleared. The next RPF-or RME-interrupt is generated by the following HDLC-frame.
1	1	RRES	HDLC-receiver is reset and the receive buffer is cleared.

3.1.4.3 Examples for the HDLC-Controller Operation

Transmission of a Frame 3 Bytes and 13 Bytes

A frame of three bytes may be entered during one serial access. The XTF $\times$ XME-command is set in the second control byte. The next XPR-status is generated after the closing flags has been transmitted successfully.

A frame of more than 4 bytes is split into groups of four or less bytes. In case of 13 bytes, for the first and the following two blocks, the XTF-bit is set in the CTRL2-register and the XBC-value contains ‘11’. The XPR-status is generated if the CPU XFIFO is ready to buffer the next part of the message. The last block of a message is indicated by setting the XTF $\times$ XME-command and the generation of XPR is delayed until the closing flag has been transmitted.

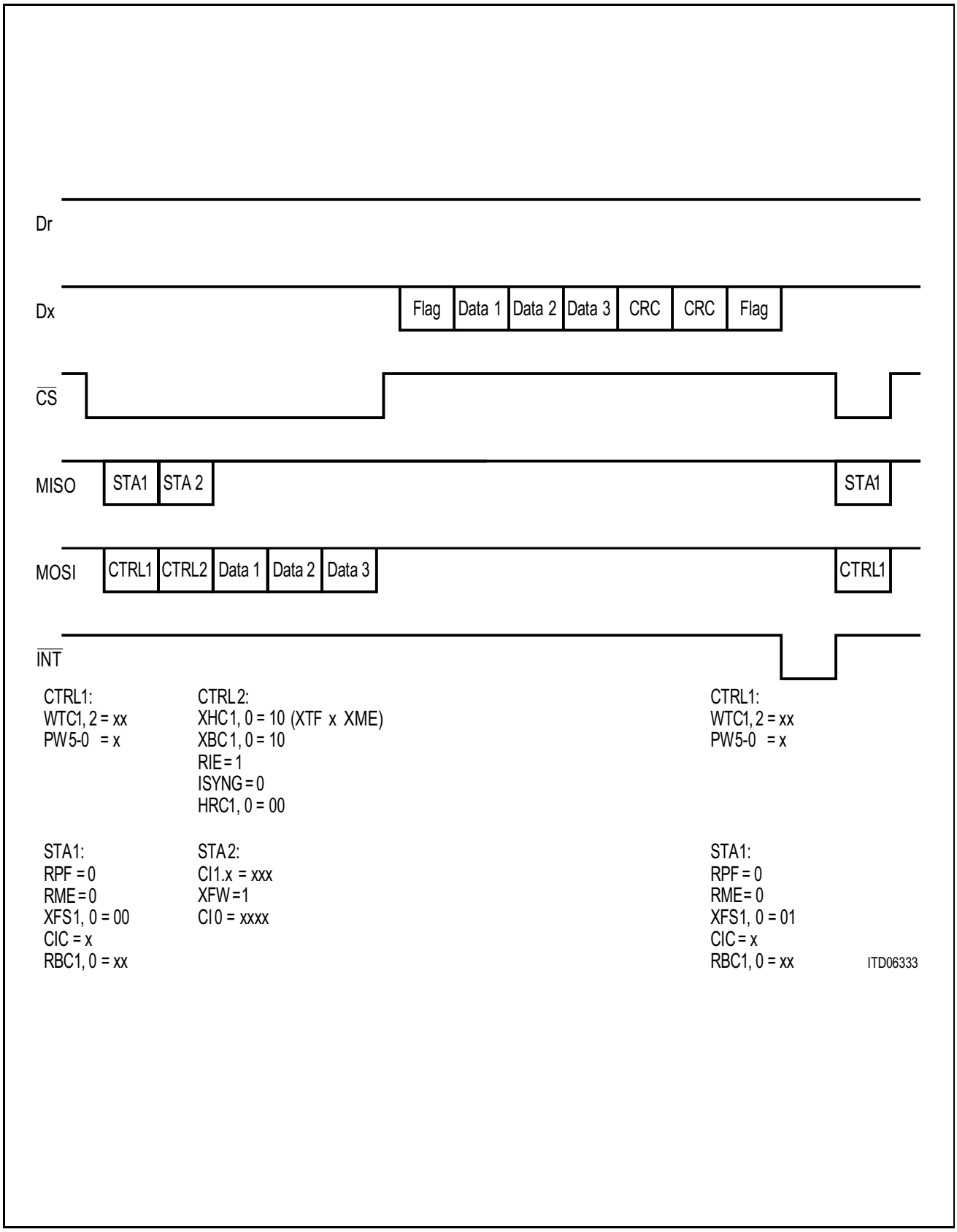


Figure 46a
Transmission of Frames

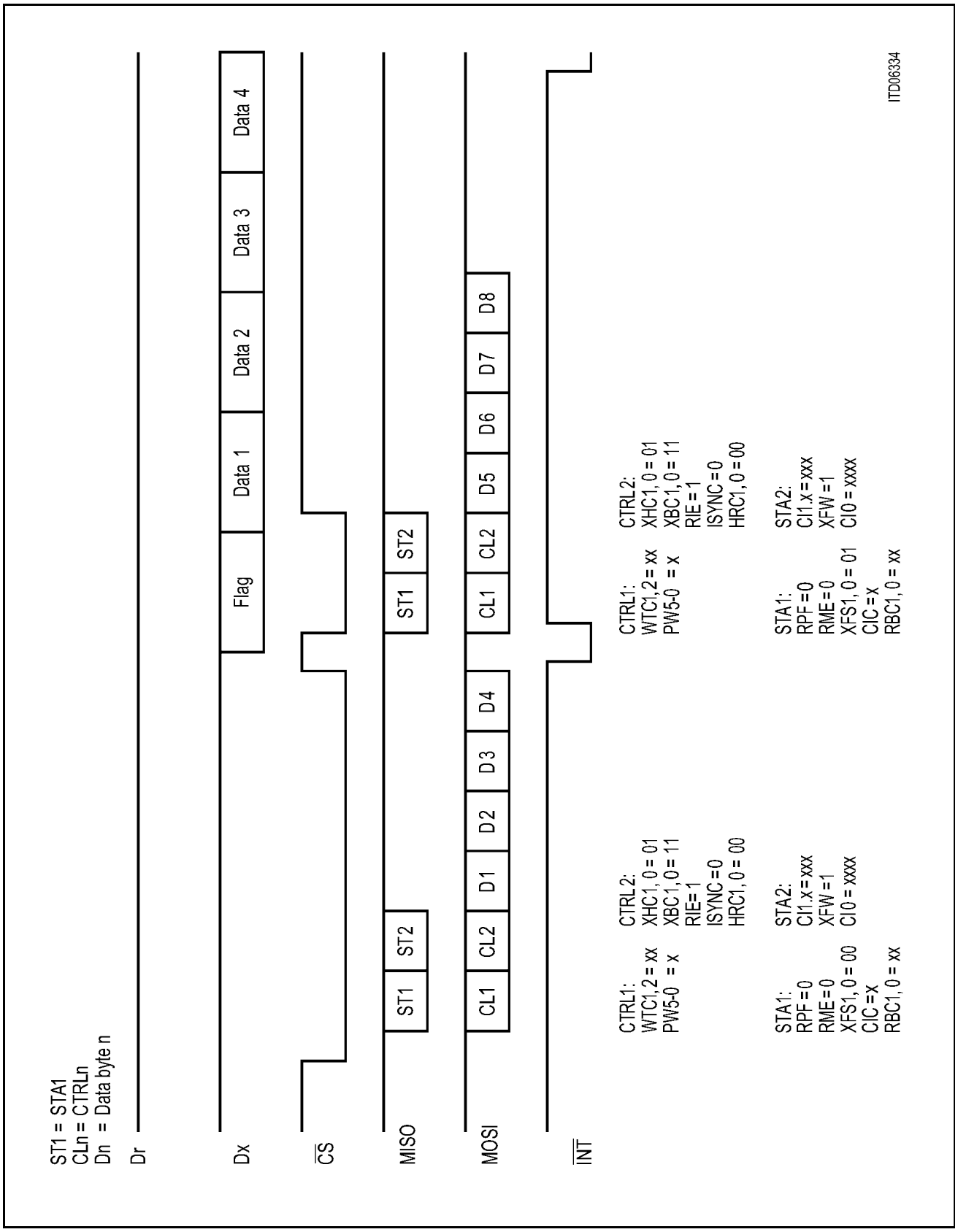


Figure 46b
Transmission of Frames

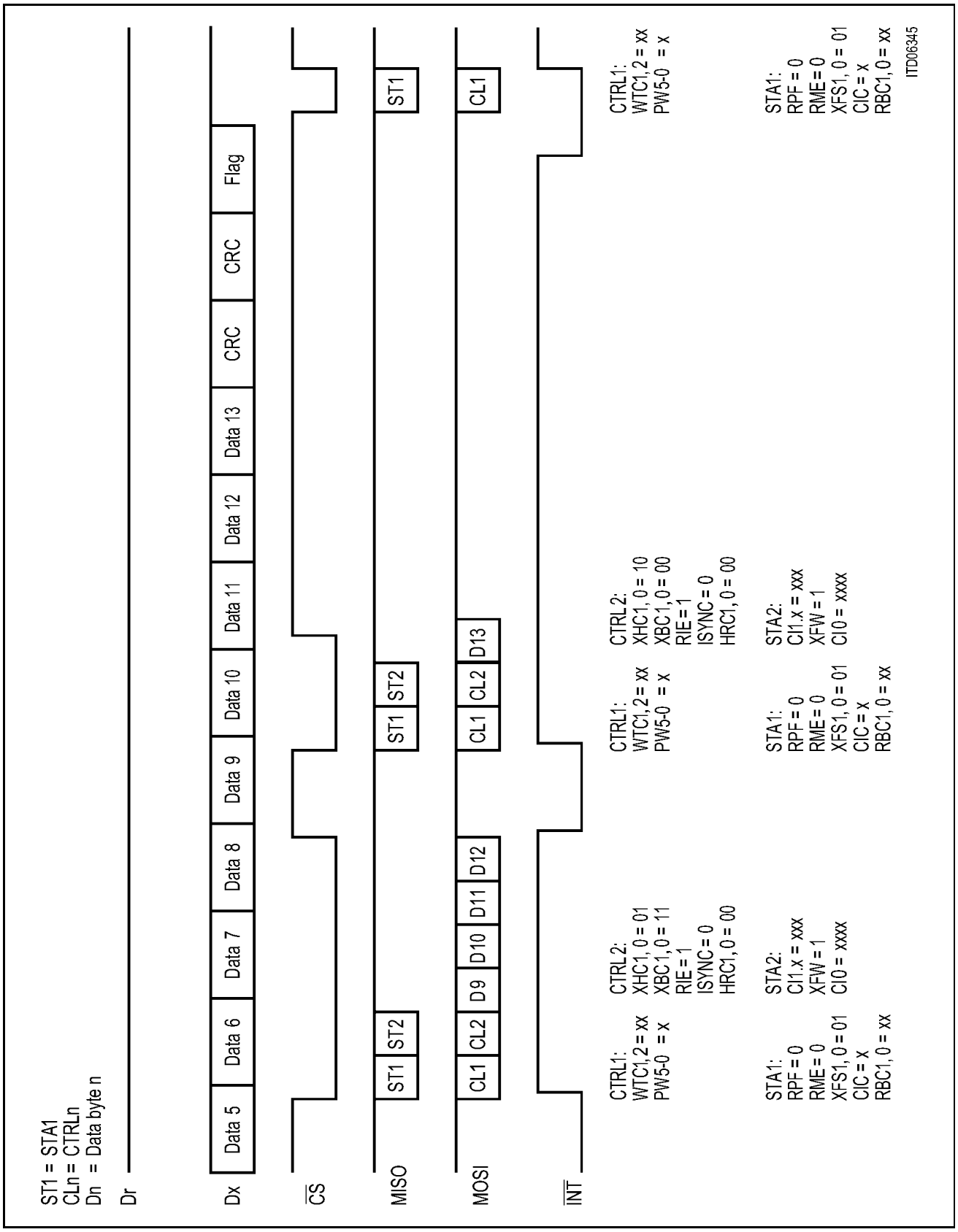


Figure 46c
Transmission of Frames

Retransmission of a Frame

In case the stop/go bit is evaluated for D-channel access control, the chances are that two terminals start transmitting at the same time and one has to abort its transmission and repeat the message. In this case, retransmission occurs automatically if the collision occurred within the first block of data. Otherwise, a XMR-status indicates that the message has to be retransmitted and therefore the data of the first block has to be written into the XFIFO.

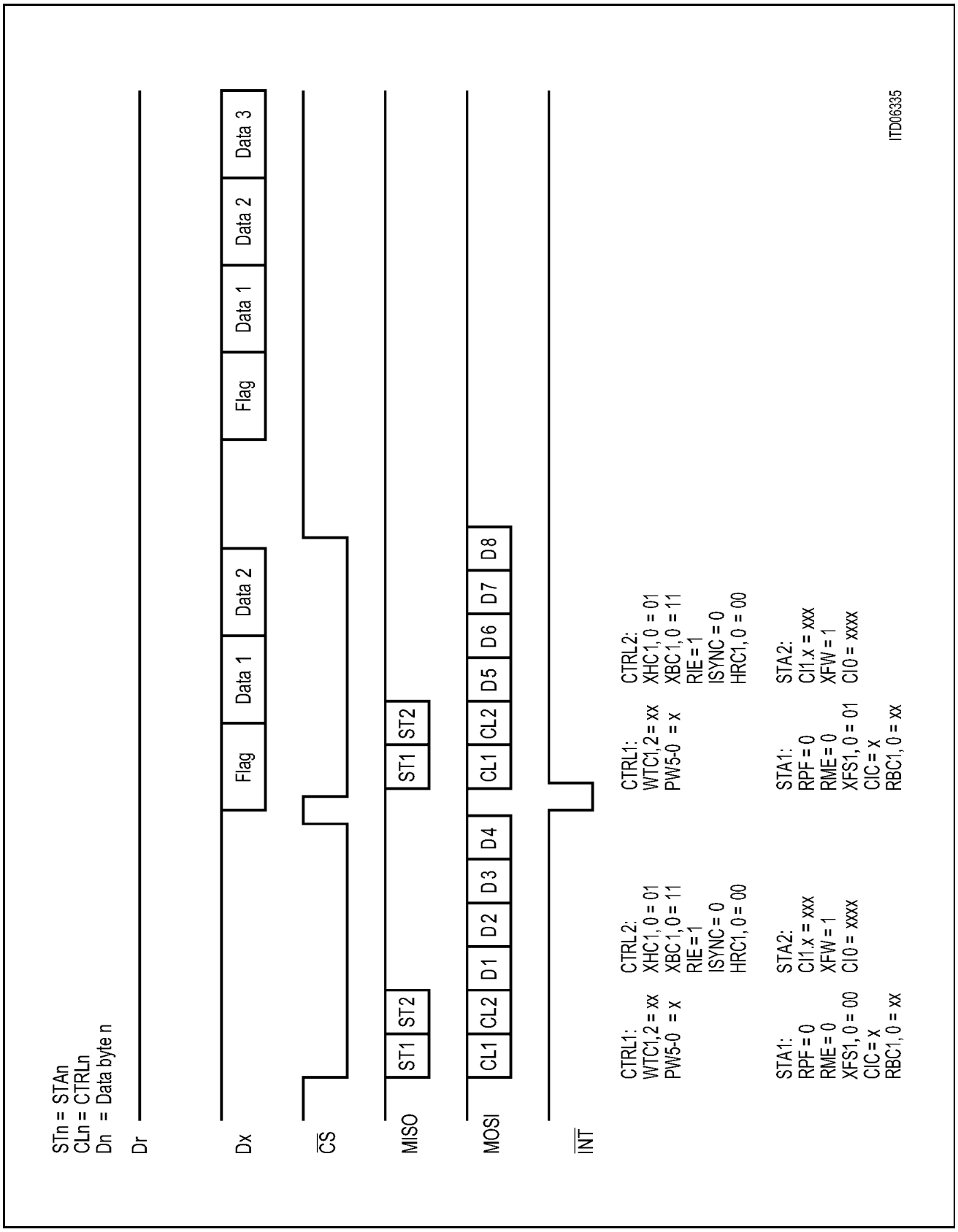


Figure 47a
Retransmission of a Frame

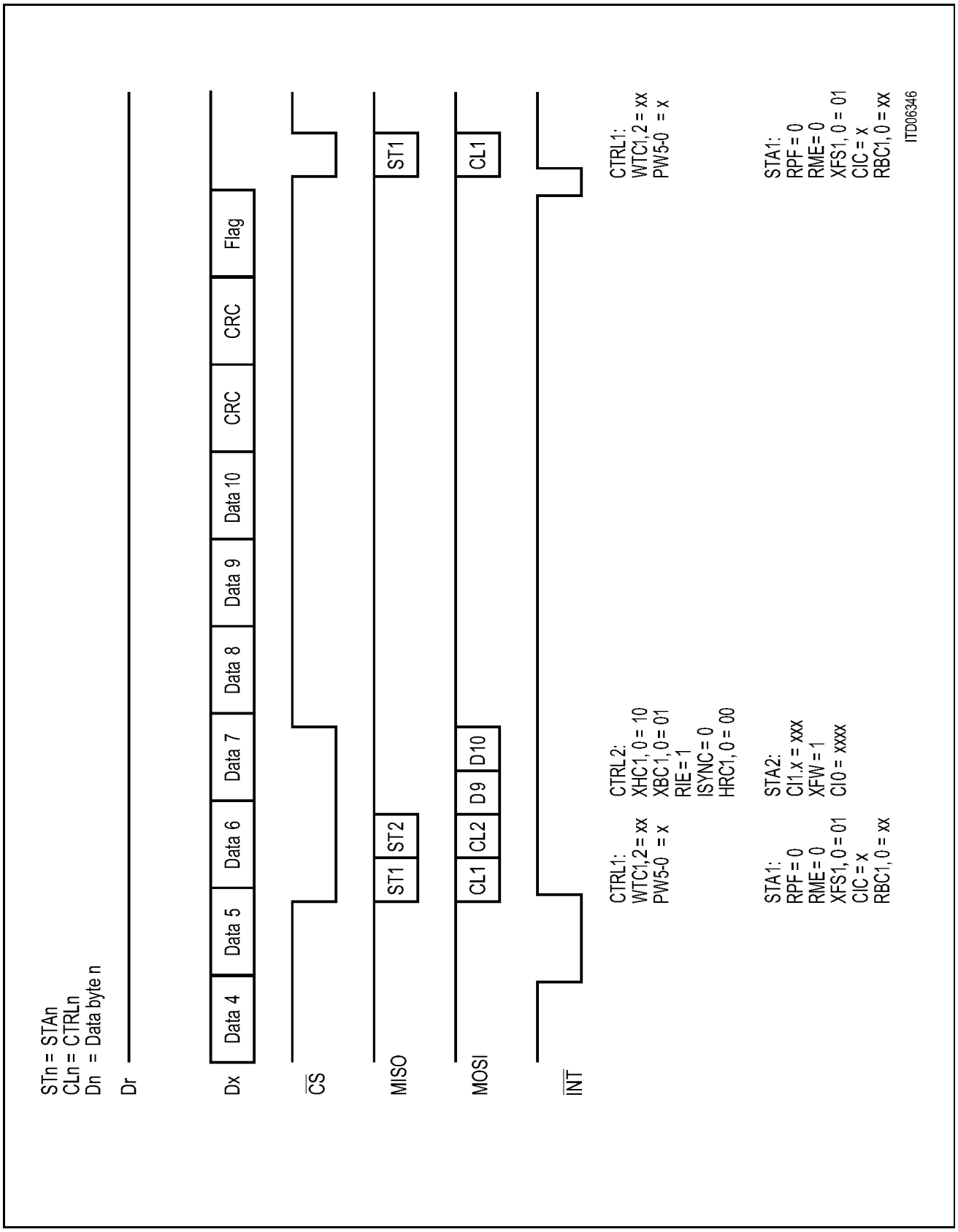


Figure 47b
Retransmission of a Frame

Transmit Data Underrun

In case the XFIFO becomes empty without detecting a XME-bit, the transmitter aborts the current frame by an abort sequence and the XDU-status is indicated.

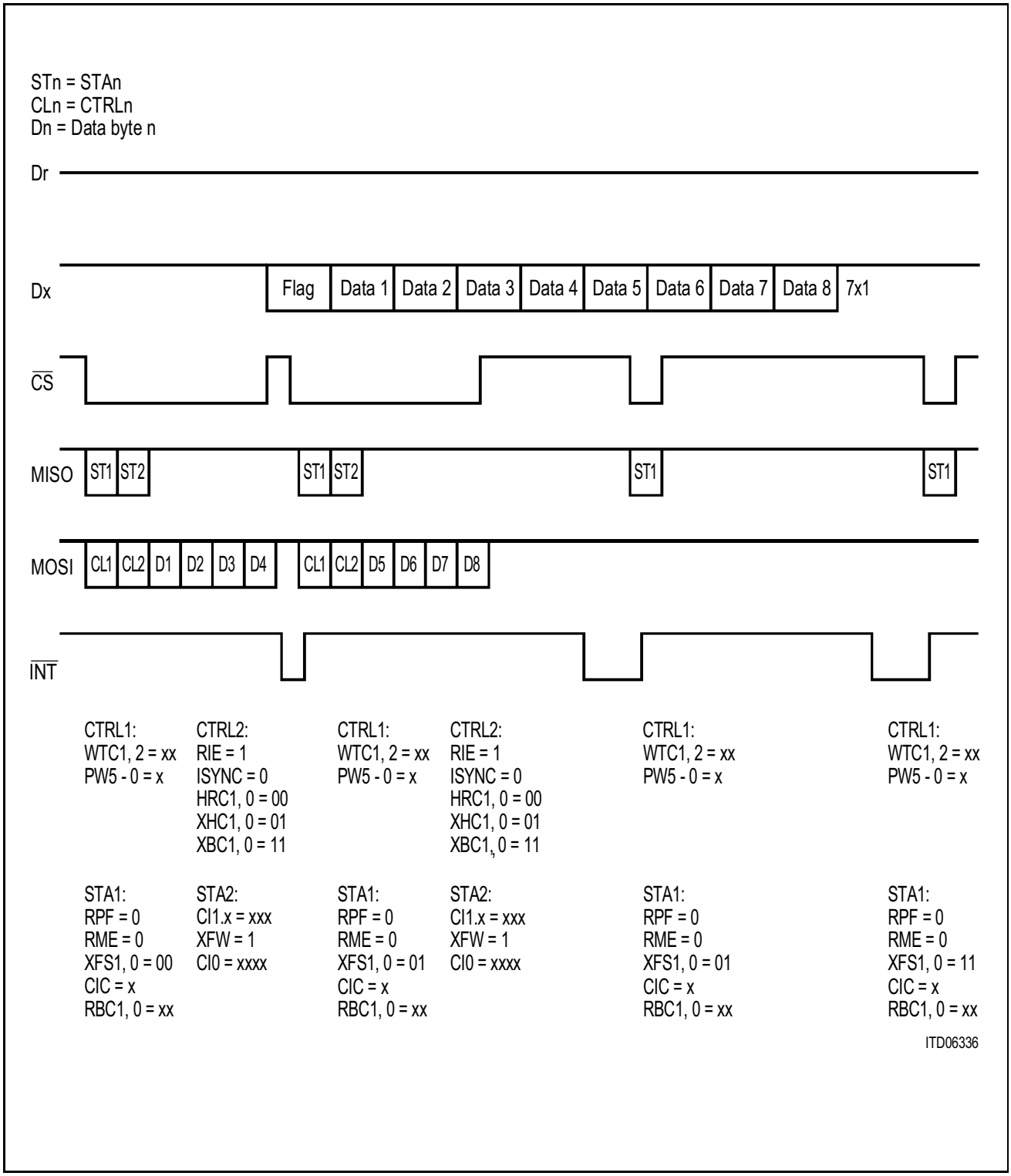


Figure 48
Transmit Data Underrun

Reception of a Frame with 3 Bytes and with 13 Bytes

The RPF- or RME-bit indicate that valid data is in the RFIFO. Both RPF- and RME-status have to be served within 2 ms to prevent an underrun condition indicated by the RDO-bit in the RSTA-value.

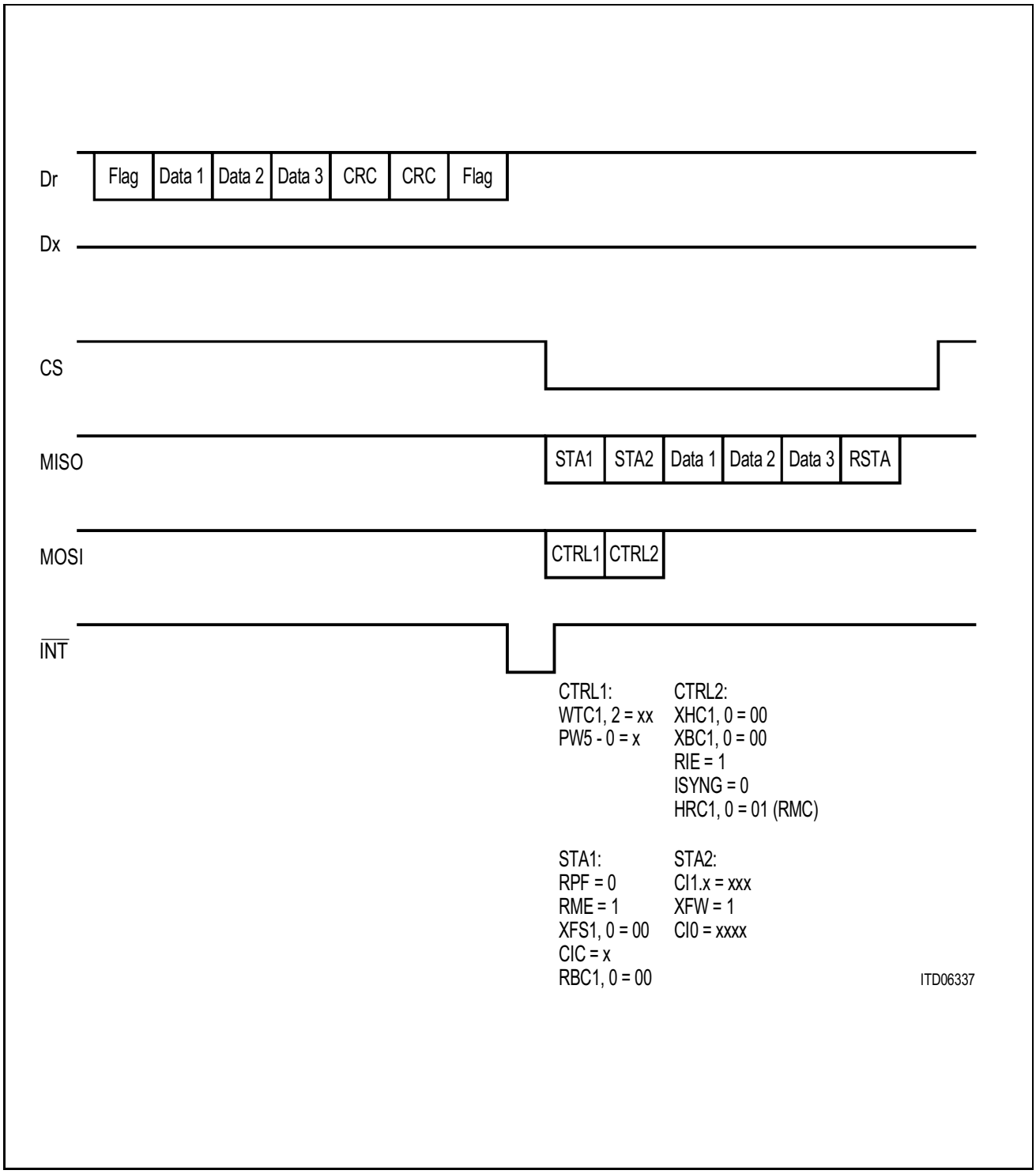


Figure 49a
Reception of Frames

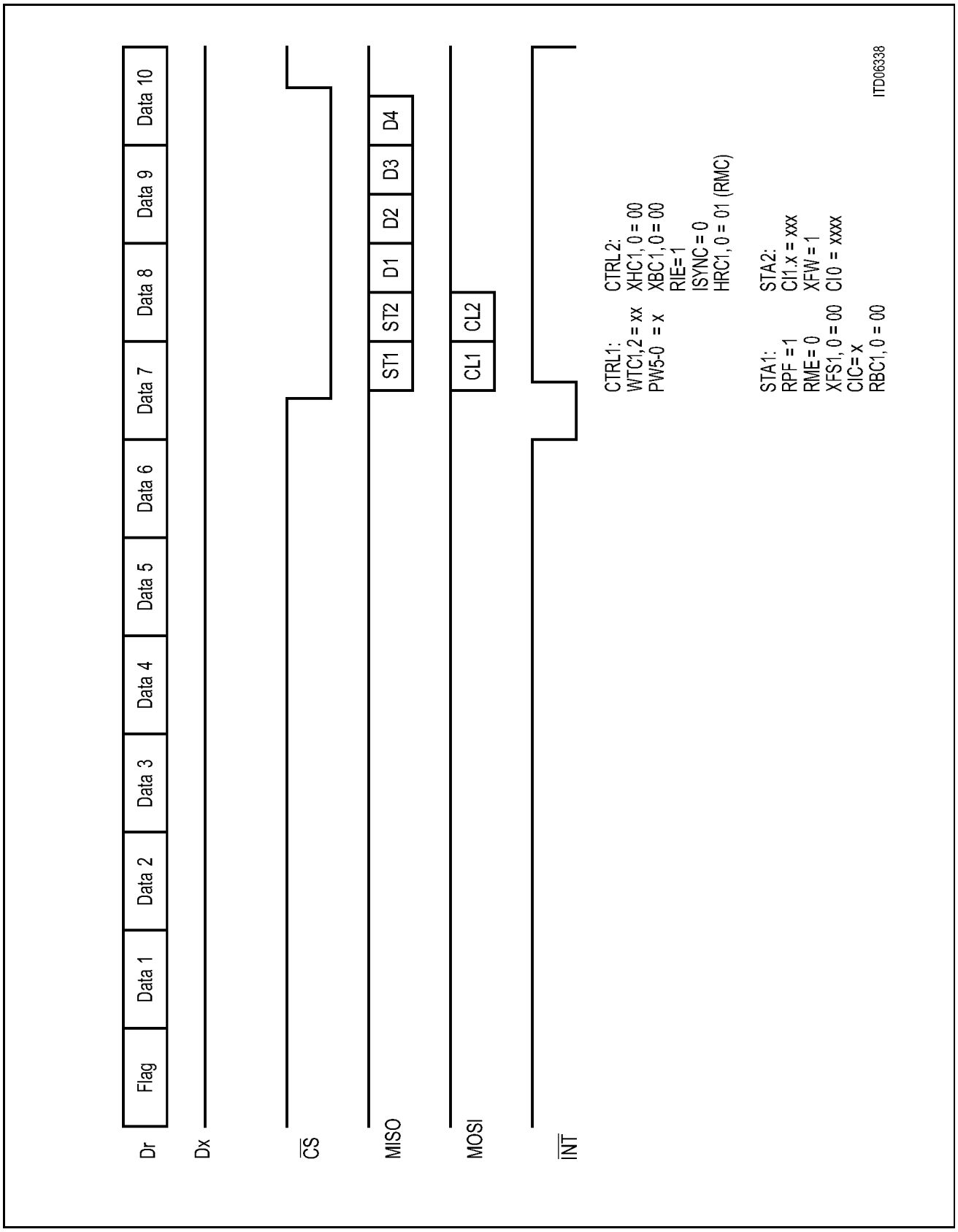


Figure 49b
Reception of Frames

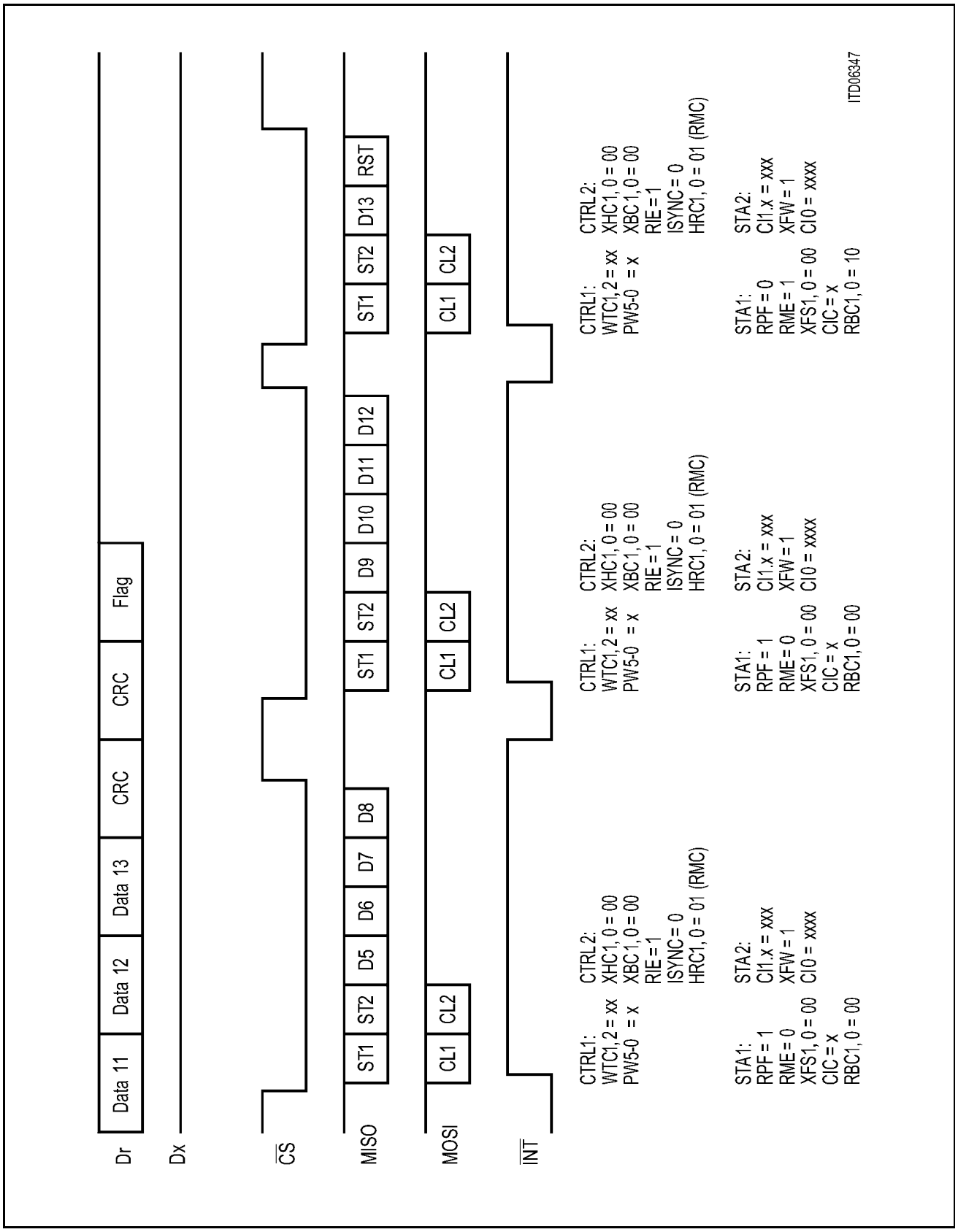


Figure 49c
Reception of Frames

Full Duplex Operation

In case of a full duplex operation where a frame is received at the same time one is transmitted, an optimization of the serial interface service is possible.

The ISYNC-bit in the CTRL2-value selects whether receive and transmit interrupts occur at any time or if the interrupt is generated only if both status bits are active.

To use the synchronization it is necessary that the third XPR-status has been indicated since this guarantees that the transmission of the frame has not been stopped within the first bytes. After the third XPR-status is detected, the ISYNC-bit may be set and the following interrupts are delayed until both a receive and transmit status is set.

After the XTF $\times$ XME-command is set or a XMR-status has been indicated it is recommended to disable the synchronous interrupt generation again.

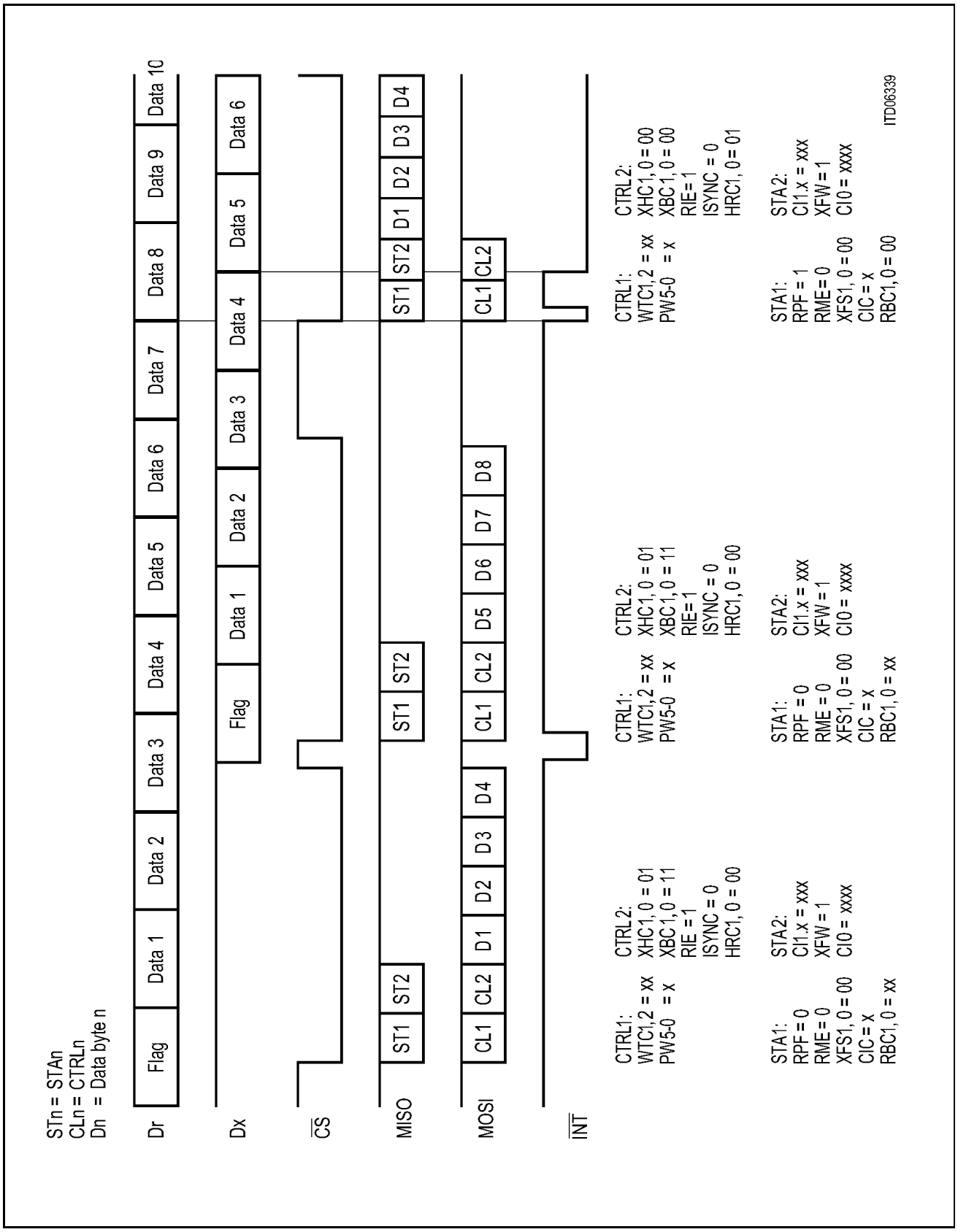


Figure 50a
Full Duplex Operation

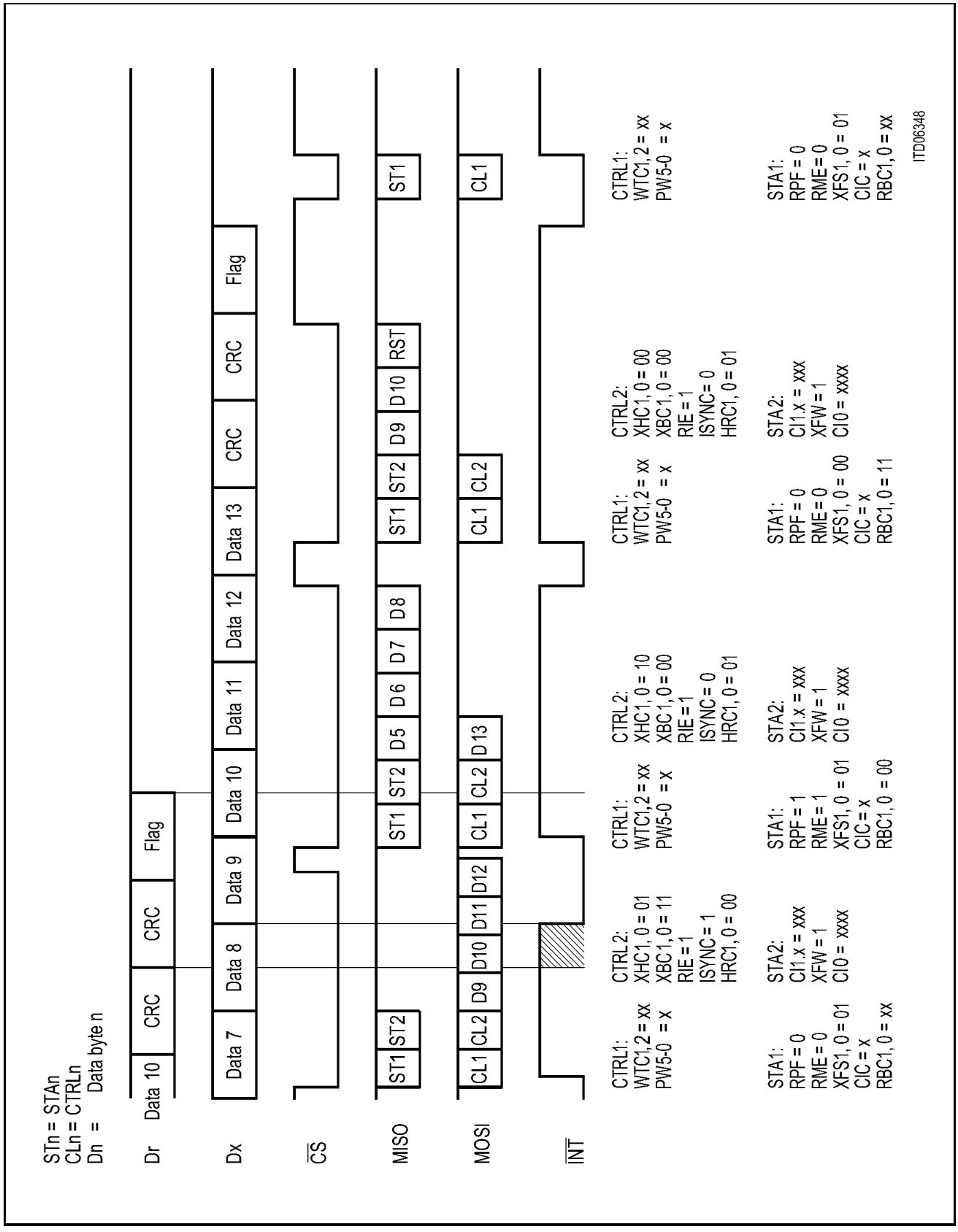


Figure 50b
Full Duplex Operation

Ignoring the Rest of a Message

The reception of a frame may be ignored after the first bytes have been read until the frame is completed. This feature is provided instead of an address recognition feature.

In this case, a RPF-interrupt indicates the first block of data and the corresponding FIFO-data is read. At the event of the next RPF-interrupt, the RMD-bit may be set in the CTRL2-value to set the corresponding command. Afterward, the next RPF- or RME-status is generated for the next frame.

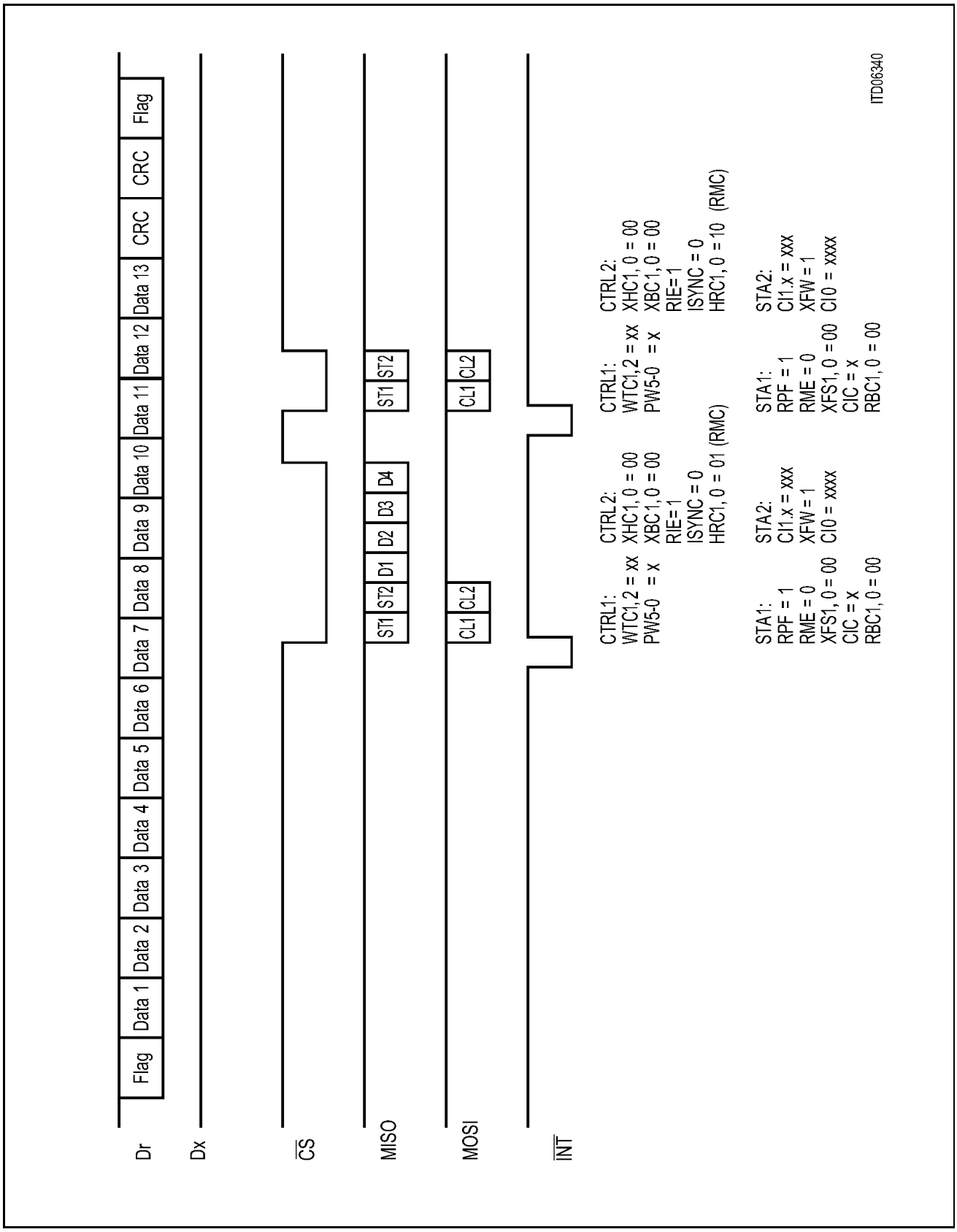


Figure 51
Ignoring the Rest of a Message

3.1.5 Reset

Reset Logic

While the power-on reset pulse is generated or an external reset is applied, pins which operate as I/O-pins are configured as inputs. The U_{pn}-awake detector becomes active after reset. IOM-clocks signals are active in TE-mode. BCL, SDS remain '0' because of the CTRL4-reset value. PWO/Ring/Mode is '0' because of the CTRL1- and CTRL3-reset values.

The registers of the SmartLink-P are reset to the default values.

Table 3
Reset State of the SmartLink-P Registers

Register	Value after Reset	Meaning
STA1	00_H	No C/I-change, no status change, no data in RFIFO.
STA2	00_H	C/I is '1111'.
CTRL1	00_H	MCLK = 3.84 MHz, Watchdog disabled, PW = '000000'.
CTRL2	00_H	No HDLC-controller operation, no XFIFO-data.
CTRL3	00_H	Permanent D-channel access, permanent access to C/I-channel 0 and D-channel. T-channel mapped on S/G, PW-output operates as LCD-contrast, TIC-bus access during D-channel transmission only, TAD = '000'.
CTRL4	00_H	Normal operation of DU-line, Serial Strobe = '000' (OFF), CI0 = '0000'.

When using the undervoltage detection for reset generation, a short internal reset is generated which resets the internal functions and starts the 56 ms counter. The IOM-clocks will be stopped after the U_{pn}-transceiver enters its deactivated state. As a result, external transceiver devices (SBCX, PSB 21810 or SmartLink in TR-mode) can not leave their reset state and they can not start activation of the IOM-2 interface. The terminal software has to enable the IOM-clocks by the SPU-bit and output the C/I-command 'RES' to guarantee a correct reset of all other transceiver devices.

3.1.6 Initialization

During initialization the control registers have to be setup. The necessary setup is listed in **table 4**.

Table 4
Initialization of the SmartLink-P Registers

Register	Bit	Effect	Application	Restricted to
CTRL1	PRE WTC PW	MCLK-clock rate Watchdog enable if required LCD-contrast value/Ringing frequency		
CTRL2	XRES RRES	Reset the HDLC-receiver and transmitter		
CTRL3	SGE, TBU SGM, BAC, TAD LCRI	Select TIC-bus, S/G-operation,T-channel mapping, TIC-bus address. LCD-contrast or ringer operation of PWM		
CTRL4	SPU CI0 SDS	Awake the IOM-interface until the received C/I-code indicates PU. Afterwards reset SPU to '0' and enter TIM or ARx in the CI0 bits. Program strobe signal		

3.2 TR-Mode

3.2.1 Control of the U_{pn}-Transceiver

3.2.1.1 Activation/Deactivation of the IOM®-2 Interface

The U_{pn}-transceiver functions are controlled by commands issued by the SmartLink-P depending on the current state. In downstream direction, only the commands 'DR', 'AR' and 'DI' trigger the state machine. In upstream direction, the four indications 'TIM', 'AR', 'AI' or 'DC' are generated.

If the IOM-2 interface is turned off, an asynchronous awake procedure is initiated if the SmartLink-P in TR-mode request an activation procedure.

In TR-mode, the length of the FSC-signal is monitored to avoid misalignment of internal buffers in case incorrect pulses on FSC have been detected. The state-machine of the U_{pn}-transceiver is reset every time, a FSC-period of less than 96 bits is detected. The SmartLink generates a reset signal for the state machine which is active for 6 IOM-frames. As a result, 4 or 5 info 0 frame will be transmitted on U_{pn} to force the TE-device in the level detect (Resynchronization) state. This number of info 0 frames is still less than is required to detect info 0 by the TE-device (2 ms, 8 info 0 frames).

3.2.1.2 Layer-1 Command/Indication Codes in TR-Mode

Command (downstream)	Abbr.	Code	Remarks
Deactivate request	DR	0000	
Activate request	AR, AI, ARL2, AIL2	1xx0	Transmission of info 2 and info 4 according to the U_{pn}-procedure
Deactivation confirmation	DC	1111	Info 0 or DI received after deactivation request or no TIC-bus request

Indication (upstream)	Abbr.	Code	Remarks
Timing	TIM	0000	Deactivation state, activation from the line not possible
Activate request	AR	1000	Info 1 received
Activate indication	AI	1100	
Deactivation indication	DI	1111	Deactivation acknowledgment, quiescent state

In TR-mode, the U_{pn}-interface is activated if the C/I-code Activate Request (AR, ARL2) or Activate Indication (AI, AIL2) has been detected in downstream direction. It stays activated until the C/I-code Deactivate Indication (DI) is received in downstream direction.

3.2.1.3 State Diagrams

In TR-mode the layer-1 (U_{pn}) part of the PSB 2197 SmartLink-P is a IOM-2 interface slave in any aspect. Therefore it is also able to activate the IOM-2 interface by pulling the data upstream line to zero asynchronously.

Since the PSB 2197 SmartLink-P in TR-mode is a stand alone function without microprocessor aid, the PSB 2197 SmartLink-P in TR-mode will indicate the activated state of the slave U_{pn}-interface by pulling bit 6 of the C/I-channel 1 on the data upstream line to ‘0’. The presence of a SmartLink-P in TR-mode is indicated by pulling bit 5 of the C/I-channel 1 on the data upstream line to ‘0’.

7							0
			CI1			MR	MX
	1/0 (activated)	0					

3.2.1.4 TR-Mode State Description

Pending Deactivation

State after reset or deactivation from the IOM-2 interface by command ‘DI’. Note that no activation from the network side is possible starting from this state.

Wait for $\overline{\text{DR}}$

This state is entered from the pending deactivation state once info 0 has been identified or after the command ‘DI’.

Deactivated

The U_{pn}-interface is deactivated and the IOM-2 interface is or will be deactivated. Activation is possible from the U_{pn}-interface and from the IOM-2 interface. If activation is initiated by the terminal side it first leads to the activation of the IOM-2 interface by the indication ‘TIM’ (Awake: DU pulled to V_{SS} asynchronously, later on synchronously).

Pending Activation 1

After activation from the line has been started the indication Activation Request (AR) is issued to get synchronization from the upstream network side.

Pending Activation 2

Upon the command Activation Request (AR) the PSB 2197 SmartLink-P transmits the 4-kHz info 2 towards the network, waiting for info 1.

Synchronized

The U_{pn}-receiver is synchronized and detects info 1. It continues the activation procedure by transmission of info 4.

Activated

The (U_{pn})-receiver is synchronized and detects info 3. The activation procedure is now completed and B1-, B2-, and downstream D-channels are conveyed transparently. For transmission of the upstream D-channel the TIC-bus function applies.

Resynchronization

Under severe disturbances on the line the U_{pn}-receiver still recognizes the receipt of a signal but is no more synchronized.

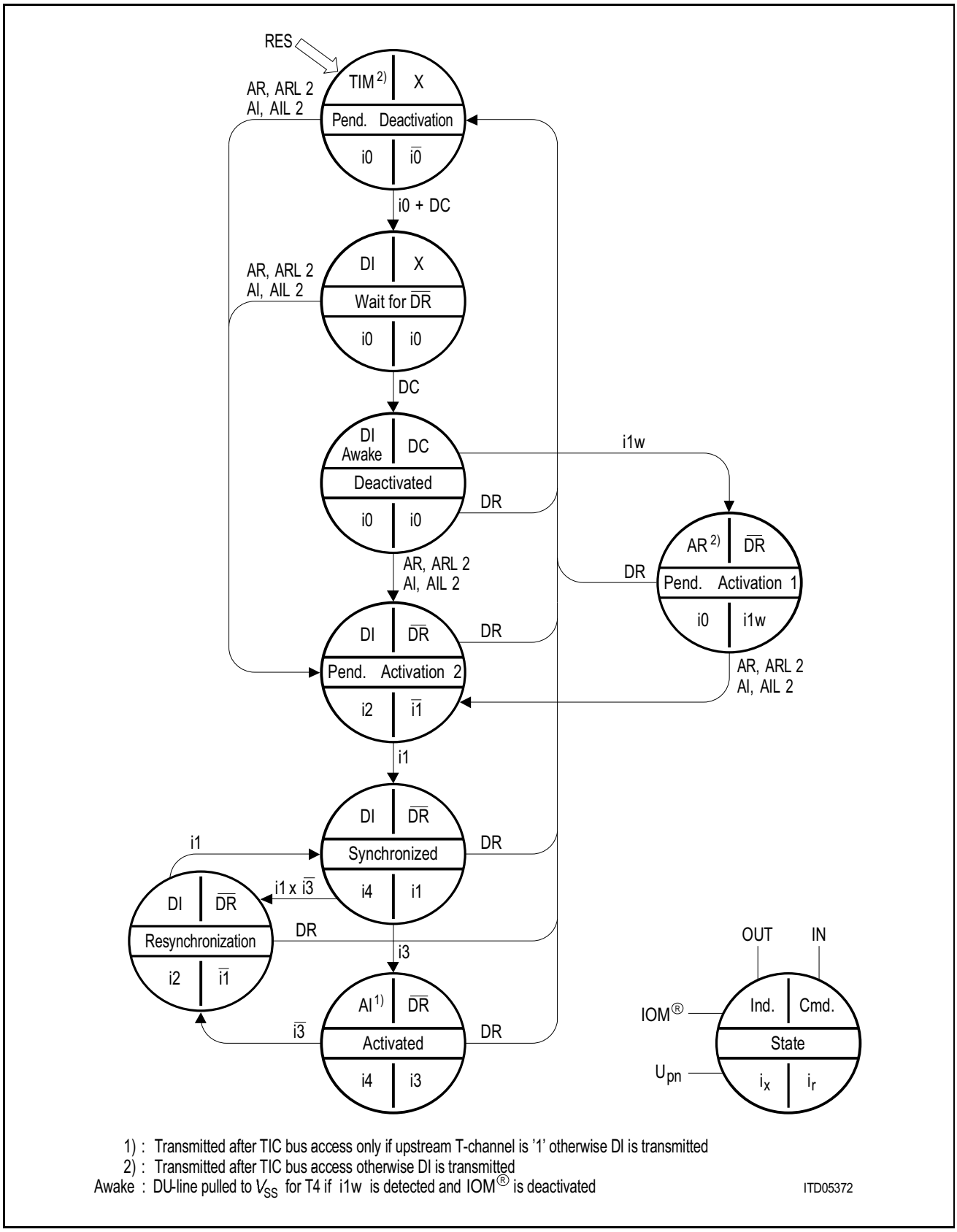


Figure 52
State Diagram TR-Mode

3.2.1.5 Example of the Activation/Deactivation

Figure 53 shows the activation/deactivation procedure between the SmartLink-P operating in TR-mode and a SmartLink-P on the slave terminal.

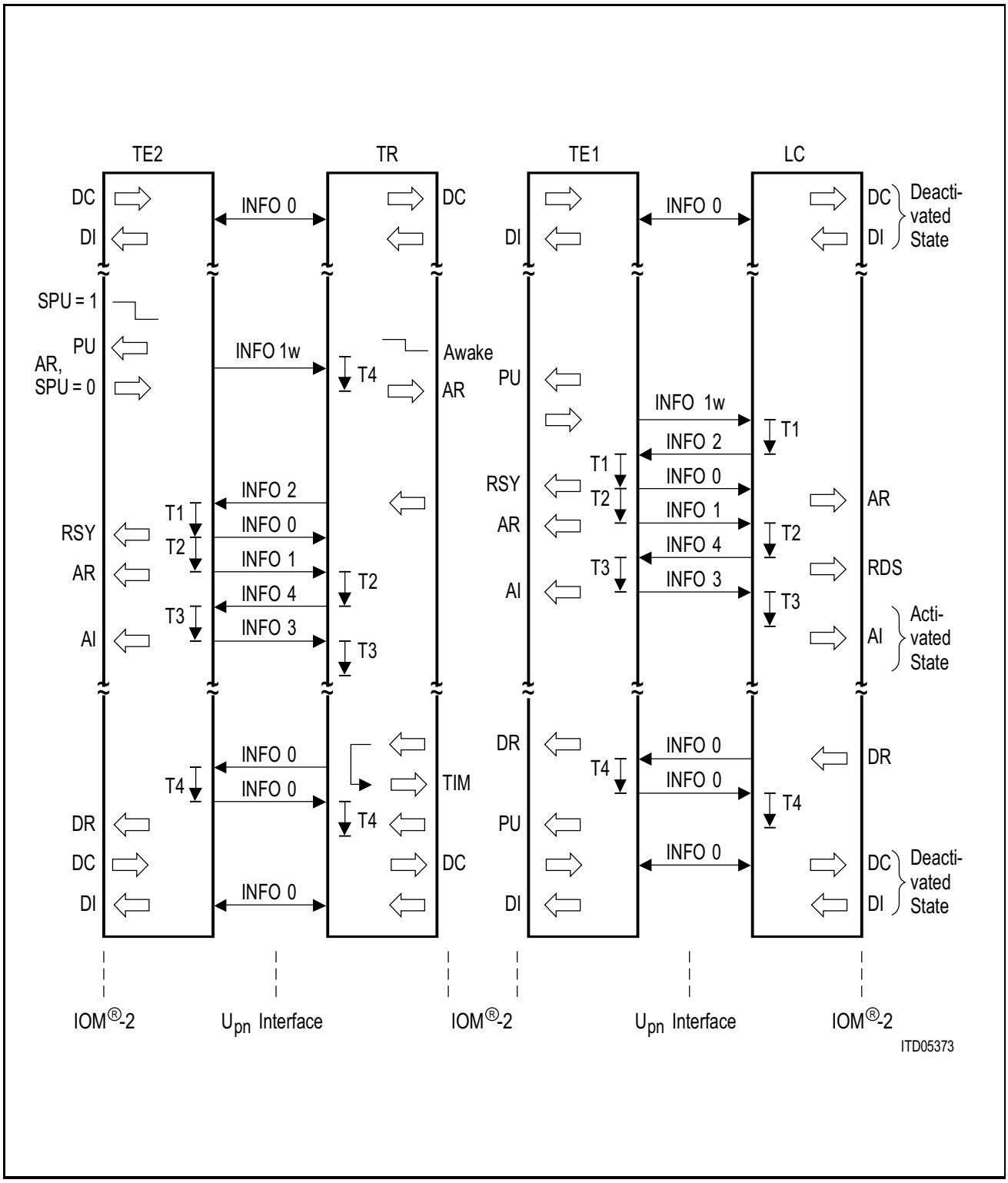


Figure 53
Activation/Deactivation (TR, TE)

3.2.2 D-Channel Access Procedure

The TR-mode uses the TIC-bus access procedure to access the upstream D-channel if requested by the terminal connected to the U_{pn}-interface.

TCM (T-Channel Mode) selects the control of the downstream T-channel source. If TCM is ‘0’, the downstream T-channel transmits the inverse value of the received stop/go bit. This is the regular operation for terminal repeater applications.

If TCM is ‘1’, the downstream T-channel is controlled by the received CI0-indication. If CI0 is different from ‘AI’ (‘1100’), the T-channel is set to ‘0’. While C/I indicates ‘AI’, the T-channel is set to permanent ‘1’. Double last look is active so that the CI0-Indications must be received twice before the T-channel changes. This mode is necessary to operate together with the IEC-Q since the IEC-Q doesn’t generate a stop/go bit so it remains ‘1’ which would indicate stop. The terminal repeater enables the T-channel after activation is completed as long as the primary link (2B1Q) is in the activated state.

TCM = ‘1’ also disables the TIC-bus access and the output of CI1 bits. The SmartLink outputs the CI0-bits and the D-bits on the DU-line permanently.

If TCM changes from ‘0’ to ‘1’ during operation, the change becomes effective immediately and a TIC-bus access is aborted. From that moment on, no further TIC-bus accesses are performed.

TIC-Bus Access (TCM = ‘0’ only)

Idle

The idle state is specified by the TIC-bus address as ‘111’ and the BAC-bit set to ‘1’. During this state, the upstream D-channel is transparent and the downstream T-bit transmits the inverse of the stop/go bit.

TIC-Bus Access by other D-Channel Sources

If the TIC-bus is occupied by another source which is indicated by the TIC-bus address different from ‘111’ or the BAC-bit set to ‘0’, the downstream T-bit changes to the block value (T = ‘0’).

TIC-Bus Request by U_{pn}-Receiver

Upon a T = ‘1’ bit received from the slave terminal which is interpreted as a D-channel access request the PSB 2197 SmartLink-P tries to access the TIC-bus according to the specified procedure using TIC-bus address ‘011’.

After the TIC-bus has been occupied the inverse of the S/G-bit position is transmitted via the U_{pn} T-bit.

If the T-channel becomes ‘0’ again, the TIC-bus is released after a delay of two IOM-2 frames. The SmartLink in TE-mode guarantees that at least one T-bit set to ‘0’ is transferred between two HDLC-frames, thus a HDLC-frame of the master can be inserted.

Blocked Condition during a Frame Transmission

If a blocked condition occurs during the transmission of a frame, the S/G-bit changes to stop and no further D-bits are output to the IOM-2 interface. The stop condition changes the downstream T-bit to a blocked state and the HDLC-transmitter in the slave terminal aborts the frame. If the upstream T-bit remains ‘0’ (BAC-bit of the terminal), the TR SmartLink-P retains its TIC-bus access to make sure that the slave terminal can transmit a frame if the stop/go bit becomes ‘Go’ again.

3.2.3 Reset State

The reset state is entered after applying an active signal to the reset input.

In reset state, the transceiver state machine is reset and info 0 is output on the U_{pn}-interface. The TIC-bus access state machine is also reset so that the TIC-bus becomes idle.

3.3 HDLC-Controller Mode

3.3.1 Interrupt Structure and Logic

The interrupt structure in HDLC-controller mode is identical to the TE-mode.

3.3.2 Control of the Serial Control Interface

The control of the serial control interface is identical to the TE-mode.

3.3.3 Control of the HDLC-Data Transfer

The control of the HDLC-data transfer is identical to the TE-mode.

3.3.4 Control of Terminal Specific Functions

Control of Upstream C/I 7 to 5

In HDLC-controller mode the control of CI1 bit 7 to 5 in upstream direction (DU) is done by the least significant three bits of CTRL1.

Generation of Bit Clock and Strobe Signals

The SDS-bits in CTRL4 control the generation of BCL-clocks and the output of the SDS-pin.

3.3.5 Reset

The reset state is identical to the TE-mode.

4 Register Description

The parameterization of the SmartLink-P and the transfer of data and control information between the microprocessor and the SmartLink-P is performed through a set of registers.

Table 5
SmartLink-P Register Map (TE)

Bit 7							Bit 0	Reg.	R/W
PRE1/ WTC1	PRE0/ WTC2	PW5	PW4	PW3	PW2	PW1	PW0	CTRL1	W
HXC1	HXC0	XBC1	XBC0	RIE	ISYNC	HRC1	HRC0	CTRL2	W
SGE	TBU	TCM	LCRI	BAC	TAD2	TAD1	TAD0	CTRL3	W
SPU	SDS2	SDS1	SDS0	CI0	CI0	CI0	CI0	CTRL4	W
								XFIFO	W
RPF	RME	XFS1	XFS0	RFO	CIC	RBC1	RBC0	STA1	R
CI1Bit7	CI1Bit6	CI1Bit5	XFW	CI0	CI0	CI0	CI0	STA2	R
								RFIFO	R
VFR	RDO	CRC	RAB	0	0	0	0	RSTA	R

SmartLink-P Register Map (HDLC-Controller Mode)

Bit 7							Bit 0	Reg.	R/W
0	0	0	0	0	CI1Bit7	CI1Bit6	CI1Bit5	CTRL1	W
HXC1	HXC0	XBC1	XBC0	RIE	ISYNC	HRC1	HRC0	CTRL2	W
SGE	TBU	TCM	0	BAC	TAD2	TAD1	TAD0	CTRL3	W
SPU	SDS2	SDS1	SDS0	CI0	CI0	CI0	CI0	CTRL4	W
								XFIFO	W
RPF	RME	XFS1	XFS0	RFO	CIC	RBC1	RBC0	STA1	R
CI1Bit7	CI1Bit6	CI1Bit5	XFW	CI0	CI0	CI0	CI0	STA2	R
								RFIFO	R
VFR	RDO	CRC	RAB	0	0	0	0	RSTA	R

4.1 SmartLink-P Register Summary

CTRL1 Control Byte 1 (TE-Mode)

Value after reset: 00_H

	Bit 7							Bit 0	Reg.	R/W
0_H	PRE1/ WTC1	PRE0/ WTC2	PW5	PW4	PW3	PW2	PW1	PW0	CTRL1	W

PRE1, 0 Prescaler Value

The PRE1, 0 bits control the microcontroller clock output. If both bits are ‘11’, the contents of PW1 and PW0 is latched and specifies the frequency.

PRE1	PRE0	PW1	PW0	MCLK-clock frequency
1	1	0	0	3.84 MHz
1	1	0	1	7.68 MHz
1	1	1	0	1.92 MHz
1	1	1	1	0.96 MHz

WTC1, WTC2 Watchdog Timer Control

During every time period of 56 ms the processor has to program the WTC1- and WTC2 bit in the following sequence to reset and restart the watchdog timer:

WTC1	WTC2
1	0
0	1

The watchdog timer is enabled by the first ‘10’ sequence. As long as both bits are ‘00’, the watchdog is not active. ‘11’ has no impact on the watchdog but controls the microcontroller clock output frequency.

PW5-0 **Pulse Width 5-0**

Specifies the output of the pulse width generator dependend on the setting of LCRI-control bit (CTRL3).

CTRL3: LCRI = 0 (LCD-contrast output)

PW5-4	PW3-0	PW output
00	0000	Off (low)
00	0001	On period: 1/15
…		
00	1110	On period: 14/15
00	1111	On (high)

PW5-4 have to be ‘00’.

CTRL3: LCRI = 1 (Ringing output)

PW5-0	Frequency
000000	PWO/Ring output is tristate
000001	8000 Hz
000010	5333 Hz
000011	4000 Hz
111110	253.96 Hz
111111	250 Hz

The value n (PW5-0) specifies a divider. The output frequency is calculated based on the following formula:

f = 16 kHz / (n + 1)

CTRL1 Control Byte 1 (HDLC-Controller Mode)

Value after reset: 00_H

	Bit 7							Bit 0	Reg.	R/W
0_H	0	0	0	0	0	CI1Bit7	CI1Bit6	CI1Bit5	CTRL1	W

Controls the bit 7 to 5 of the command/indicate channel 1 on data upstream.

CI1Bit7

0: CI1Bit7 = 1

1: CI1Bit7 = 0

CI1Bit6

0: CI1Bit6 = 1

1: CI1Bit6 = 0

CI1Bit5

0: CI1Bit5 = 1

1: CI1Bit5 = 0

CTRL2 Control Byte 2

Value after reset: 00_H

	Bit 7							Bit 0	Reg.	R/W
1_H	HXC1	HXC0	XBC1	XBC0	RIE	ISYNC	HRC1	HRC0	CTRL2	W

Note: The HDLC-controller operates on DCL/2 clock rate. It requires 4 clock cycles to execute a command entered in the CTRL2-register. After a FIFO-part has been transferred, the corresponding interrupt is generated immediately.

HXC1, 0 HDLC-Transmitter Control 1, 0

HXC provides the commands for the HDLC-transmitter:

HXC1	HXC0	Command
0	0	No command, XBC selects whether CTRL3 and 4 is transmitted
0	1	XTF, Transmit Transparent Frame. XBC determines the number of valid, XFIFO-bytes to follow.
1	0	XTF $\times$ XME, Transmit Transparent Frame and Transmit Message End. XBC determines the number of valid XFIFO-bytes to follow.
1	1	XRES, Transmitter Reset

XBC1, 0 Transmit Byte Count 1, 0

Indicates the number of valid bytes for the XFIFO which follow after the control bytes if HXC1, 0 is not ‘00’.

XBC1	XBC0	Transmit Byte Count
0	0	1 Byte
0	1	2 Bytes
1	0	3 Bytes
1	1	4 Bytes

If HXC1, 0 = ‘00’, XBC1, 0 selects whether CTRL3 and CTRL4 are transmitted after CTRL2.

XBC1	XBC0	
0	0	No valid data follows after CTRL2.
0	1	CTRL3 and CTRL4 follow after CTRL2.

RIE **Receiver Interrupt Enable**

RIE controls the generation of receive interrupts.

0: Receiver interrupts are masked.

1: Receiver interrupts are enabled. An interrupt is generated if four bytes are valid in the RFIFO (RPF) or if the RME-bit is set.

ISYNC **Interrupt Synchronization**

Used to synchronize transmit and receive interrupts to allow simultaneous access to the XFIFO and RFIFO.

0: RPF-, RME- and XFS-interrupt generation is not synchronized.

1: An interrupt is generated only if both a receive interrupt (RPF, RME) and a transmit interrupt (XFS1, XFS0) is active.

HRC1, 0 **HDLC Receiver Control 1, 0**

HRC provides the commands for the HDLC-receiver:

HRC1	HRC0	Command
0	0	No command
0	1	RMC, Receive Message Complete
1	0	RMD, Receive Message Delete
1	1	RRES, Receiver Reset

CTRL3 Control Byte 3

Value after reset: 00_H

	Bit 7							Bit 0	Reg.	R/W
2_H	SGE	TBU	TCM	LCRI	BAC	TAD2	TAD1	TAD0	CTRL3	W

SGE Stop/Go Bit Evaluation

Specifies whether the S/G-bit is evaluated for D-channel transmission.

0: Permanent D-channel transmission.

1: D-channel transmission only during S/G = ‘go’.

TBU TIC-Bus Used

Specifies whether the TIC-bus procedure is used to gain access to the C/I-channel 0 and D-channel.

0: Permanent access to the C/I-channel 0 and D-channel.

1: TIC-bus procedure is used to access the upstream C/I-channel 0 and D-channel. The TIC-bus address is specified in bit 0 to 2.

TCM T-Channel Mapping

0: T-channel data is mapped onto the S/G-bit (S/G = inverse T-channel).

1: T-channel data is mapped onto the AB-bit (AB = T-channel).

LCRI LCD-Contrast/Ringing Output (used in TE-Mode only)

0: Pulse width output operates as LCD-contrast output. PW-0 specifies the on-to-off ratio of a fixed frequency signal. PW5-4 have to be ‘00’.

1: Pulse width output operates as ringing output. PW5-0 specifies the ringing frequency.

BAC TIC-Bus Access

Forces the SmartLink-P to occupy the TIC-bus without transmission of D-channel data. Valid only if TBU is ‘1’.

0: TIC-bus used for D-channel data transmission only.

1: TIC-bus accessed permanently.

TAD2-0 **TIC-Bus Address**

Specifies the TIC-bus address used by the SmartLink-P.

TAD2	TAD1	TAD0	TIC-bus address
0	0	0	0 (highest priority)
0	0	1	1
0	1	0	2
…			
1	1	0	6
1	1	1	7 (lowest priority)

CTRL4 Control Byte 4

Value after reset: $0F_H$

	Bit 7							Bit 0	Reg.	R/W
3_H	SPU	SDS2	SDS1	SDS0	CI0	CI0	CI0	CI0	CTRL4	W

SPU Software Power-Up

0: Normal operation of DU.

1: DU is pulled low while SPU = '1'. Used to awake the IOM-interface.

SDS2-0 Serial Data Strobe

Controls the generation of the serial data strobe signal and the BCL-signal. SDS2-0 also specify whether B-channel information is looped or the upstream B-channel information is muted.

SDS2	SDS1	SDS0	Function of SDS	Upstream Time-Slot Data
0	0	0	SDS low, BCL low	Transparent
0	0	1	SDS high during IC1, BCL active	Transparent
0	1	0	SDS high during B1, BCL active	Transparent
0	1	1	SDS high during B2, BCL active	Transparent
1	0	0	SDS low, BCL low	Downstream B1 looped to upstream B1
1	0	1	SDS low, BCL low	Downstream B2 looped to upstream B2
1	1	0	SDS high during B1, BCL active	Upstream B1 muted
1	1	1	SDS high during B2, BCL active	Upstream B2 muted

B-Channel Looping

During the B-channel loop selected by the SDS-bits, the received B-channel data from the U_{pn}-interface is output on the DD-line and looped back to the DU-line. The DU-line is not disconnected which means that the external components on the DU-line must output ‘FF’ during the B-channel time-slot which is looped back. Otherwise the information is ‘ored’ in terms of a ‘0’ bit overwriting a ‘1’ bit. The advantage of this method is that monitoring is possible on the IOM-interface pins.

B-Channel MUTE

While the B-channel MUTE function is active, the connection between the external DU-line and the internal B-channel input line is disconnected and the B-channel input sees only ‘1’s. The DU-line will still show the output of the codec but the U_{pn}-B-channel information is ‘FF’. This implementation provides no easy method to check the MUTE function since the B-channel information is scrambled before it is transmitted on the U_{pn}-interface.

CI0 **Command/Indicate Channel 0**

Value which is transmitted on the upstream C/I-channel 0 depending on the BAC and TBU bit.

STA1 Status Byte 1

Value after reset: 00_H

	Bit 7							Bit 0	Reg.	R/W
0_H	RPF	RME	XFS1	XFS0	RFO	CIC	RBC1	RBC0	STA1	R

RPF Receive Pool Full

Indicates that a part of a message is stored in the RFIFO. All four bytes contain valid data.

RME Receive Message End

Indicates that the last part of a message is stored in the RFIFO. The RBC1, 0-value indicates the number of valid bytes in the RFIFO. This number includes the RSTA-value.

XFS1, XFS0 Transmit FIFO-Status

Indicates the status of the transmit FIFO.

XFS1	XFS0	Appr.	Transmit FIFO-Status
0	0		No change in the transmit FIFO-status.
0	1	XPR	Transmit Pool ready. Up to four bytes may be entered.
1	0	XMR	Transmit message repeat. The S/G-bit became stop and the frame has to be reentered. Up to four bytes may be entered.
1	1	XDU	Transmit Data Underrun. The transmitter became empty without XME-marking. The frame is aborted (7 ‘1’). The XFIFO is cleared and new data may be entered.

The generation of the XPR-status is delayed until the closing flag has been transmitted completely if the previous transmitter command was XME.

RFO Receive Frame Overflow

The begin of an HDLC-frame (1st byte) could not be stored since the RFIFO is full.

CIC **C/I-Code Change**

Indicates that a new C/I-code is available in STA2.

0: No C/I-code change

1: C/I-code change occurred. The new value is stored in the STA2-register.

RBC1, 0 **Receive Byte Count**

Indicates the number of valid bytes in the RFIFO if a RME-status bit is set to '1'. This value is repeated while STA1 is read until the RMC, RMD or RRES is issued. It is not changed by reading the RFIFO.

RBC1	RBC0	Number of valid bytes in the RFIFO
0	1	1 Byte
1	0	2 Byte
1	1	3 Byte
0	0	4 Byte

If RME or RPF is '0', the RBC1, 0-values may have any value and should be ignored by the software.

STA2 **Status Byte 2**

Value after reset: $0F_H$

	Bit 7							Bit 0	Reg.	R/W
1_H	CI1Bit7	CI1Bit6	CI1Bit5	XFW	CI0	CI0	CI0	CI0	STA2	R

CI1Bit7 **C/I-Channel 1 Bit 7**

Indicates the state of bit 7 on the upstream C/I-channel 1. This bit is reserved to indicate the presence of a SmartLink-S in LT-S mode.

0: C/I-channel 1 bit 7 is ‘0’ (SmartLink-S present)

1: C/I-channel 1 bit 7 is ‘1’ (SmartLink-S not present)

CI1Bit6 **C/I-Channel 1 Bit 6**

Indicates the state of bit 6 on the upstream C/I-channel 1 to indicate the active state of the slave U_{pn}-interface.

0: C/I-channel 1 bit 6 is ‘0’ (Slave U_{pn} activated)

1: C/I-channel 1 bit 6 is ‘1’ (Slave U_{pn} not activated)

CI1Bit5 **C/I-Channel 1 Bit 5**

Indicates the state of bit 5 on the upstream C/I-channel 1 to detect the presence of the slave U_{pn}-interface.

0: C/I-channel 1 bit 5 is ‘0’ (TR SmartLink-P present)

1: C/I-channel 1 bit 5 is ‘1’ (TR SmartLink-P not present)

XFW **Transmit FIFO Write Enable**

Indicates that the XFIFO is able to receive new data. XFW is a static indication. It changes its state after a transmit command has been executed internally or if the XFIFO becomes empty.

0: XFIFO is not empty

1: XFIFO is empty. The next part of the frame or a new frame may be entered.

The generation of the XFW-status bit is delayed until the closing flag has been transmitted completely if the previous transmitter command was XME.

CI0 **C/I-Code 0**

Indicates the received (downstream) C/I-code of channel 0.

RSTA **Receiver Status Byte**

Bit 7							Bit 0	Reg.	R/W
VFR	RDO	CRC	RAB	0	0	0	0		

VFR **Valid Frame**

Indicates that the frame consists of multiples of 8 bits and the minimum number of bytes between two flags was 3.

RDO **Receive Data Overflow**

Indicates that the RFIFO was not serviced in time and that at least one byte of the message could not be stored.

0: No data lost

1: At least one byte lost

CRC **CRC-Check Correct**

Indicates whether a CRC-check was okay or not.

0: CRC error

1: CRC okay

RAB **Receiver Abort**

Indicates that the frame was not closed by a flag but by an abort sequence (7 ‘1’).

0: Frame closed with flag

1: Frame closed with abort sequence

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Voltage on any pin with respect to ground	V_S	– 0.4 to V_{DD} + 0.4	V
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	– 65 to 125	°C

DC-Characteristics

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition	Remarks
		min.	typ.	max.			
L-input voltage	V_{IL}	– 0.4		0.8	V		All pins except Lla, Llb
H-input voltage	V_{IH}	2.0		V_{DD} + 0.4	V		All pins except Lla, Llb
L-output voltage L-output voltage 1	V_{OL} V_{OL1}			0.45 0.45	V V	I_{OL} = 2 mA I_{OL} = 7 mA (DD, DU only)	All pins except Lla, Llb
H-output voltage	V_{OH} V_{OH1}	2.4 V_{DD} – 0.5			V V	I_{OH} = – 400 µA I_{OH} = – 100 µA	All pins except Lla, Llb, MISO
H-output voltage	V_{OH}	V_{DD} – 0.5			V	I_{OH} = – 1 mA	MISO

DC-Characteristics (cont'd)
T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition	Remarks
		min.	typ.	max.			
Power supply current TE-mode operating	I_{CC}		10	15	mA	DCL = 1.536 MHz	V_{DD} = 5 V inputs at V_{SS}/V_{DD}, no output loads except Lla, Llb; Lla, Llb load ± 15 mA
TE-mode deactivated, IOM-clocks stopped	I_{CC}		9		mA	DCL = 0 MHz	V_{DD} = 5 V inputs at V_{SS}/V_{DD}, no output loads.
TR-mode operating	I_{CC}		8.5		mA	DCL = 1.536 MHz	V_{DD} = 5 V inputs at V_{SS}/V_{DD}, no output loads except Lla, Llb; Lla, Llb load ± 15 mA
TR-mode deactivated, IOM stopped	I_{CC}		7.5		mA	DCL = 0 MHz	V_{DD} = 5 V inputs at V_{SS}/V_{DD}, no output loads.
HDLC controller mode	I_{CC}		4.5		mA	DCL = 1.536 MHz	V_{DD} = 5 V inputs at V_{SS}/V_{DD}, no output loads.
Input leakage current Output leakage current	I_{LI} I_{LO}			10 10	µA µA	0 V < V_{IN} < V_{DD} 0 V ≤ V_{OUT} ≤ V_{DD}	All pins except Lla, Llb
Transmitter output impedance		10		30	Ω	I_{OUT} = 20 mA	Lla, Llb
Receiver input impedance		10			kΩ	V_{DD} = 5 V transmitter inactive	Lla, Llb

DC-Characteristics (cont'd)
T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition	Remarks
		min.	typ.	max.			
H-input voltage L-input voltage	V_{IH} V_{IL}	3.5 – 0.4		V_{DD} + 0.4 1.5	V V		XTAL1 XTAL1
H-output voltage L-output voltage	V_{OH} V_{OL}	4.5		 0.4	V V	I_{OH} = 100 µA $C_I \leq$ 60 pF I_{OL} = 100 µA $C_I \leq$ 60 pF	XTAL2 XTAL2

Capacitances
T_A = 0 to 70 °C; V_{DD} = 5 V ± 5 %, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input capacitance I/O-capacitance	C_{IN} $C_{I/O}$		7 7	pF pF	All pins except Lla, Llb
Output capacitance	C_{OUT}		25	pF	Lla, Llb
Load capacitance	C_I		60	pF	XTAL1, XTAL2

Oscillator Circuits

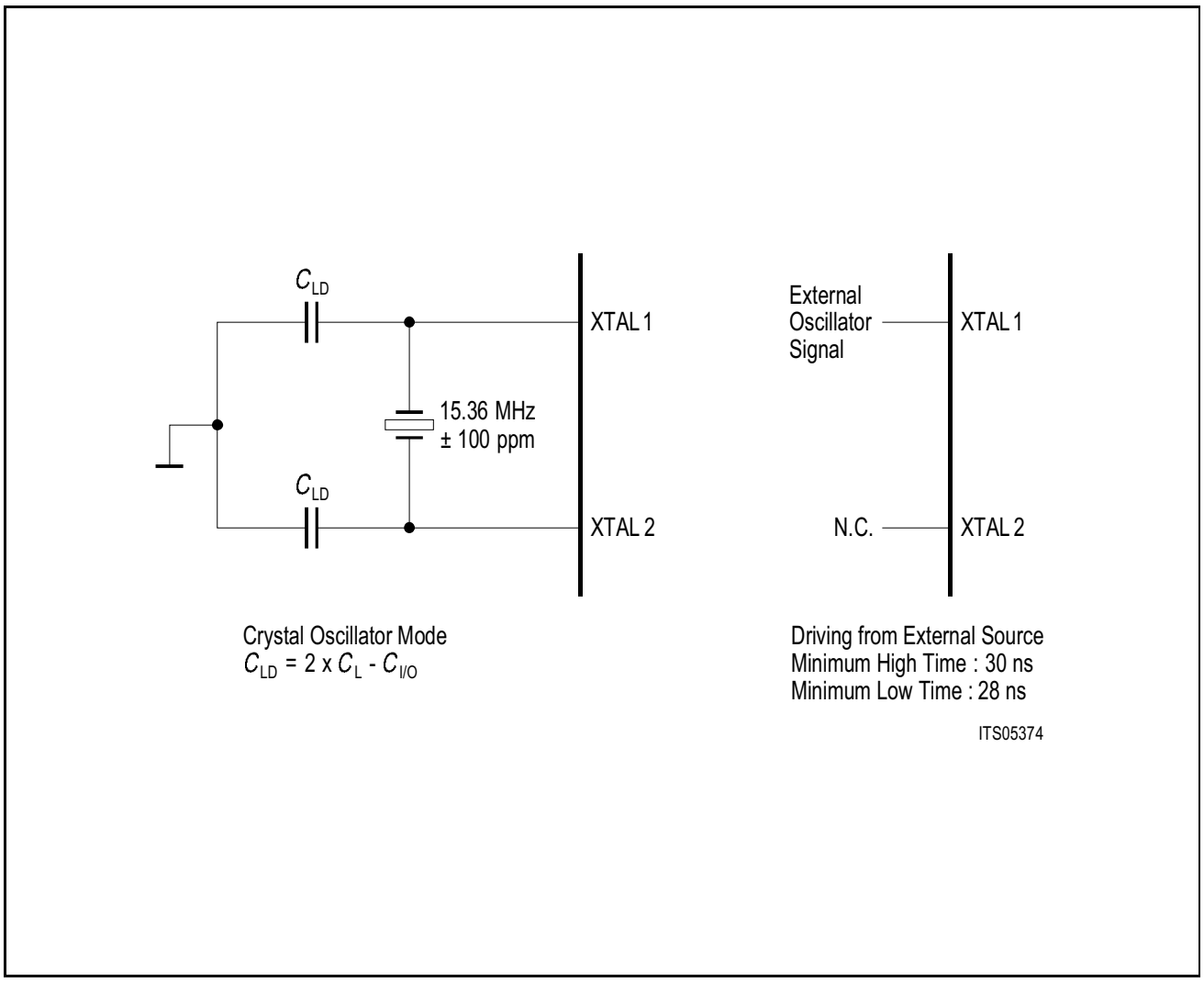


Figure 54
Oscillator Circuits

XTAL1, 2 Recommended **typical** crystal parameters.

Parameter	Symbol	Limit Values		Unit
Motional capacitance	C_1	20		fF
Shunt	C_0	7		pF
Load	C_L	≤ 30		pF
Resonance resistor	R_r	≤ 65		Ω

AC-Characteristics

Inputs are driven to 2.4 V for a logical ‘1’ and to 0.45 V for a logical ‘0’. Timing measurements are made at 2.0 V for a logical ‘1’ and 0.8 V for a logical ‘0’. The AC testing input/output waveforms are shown below.

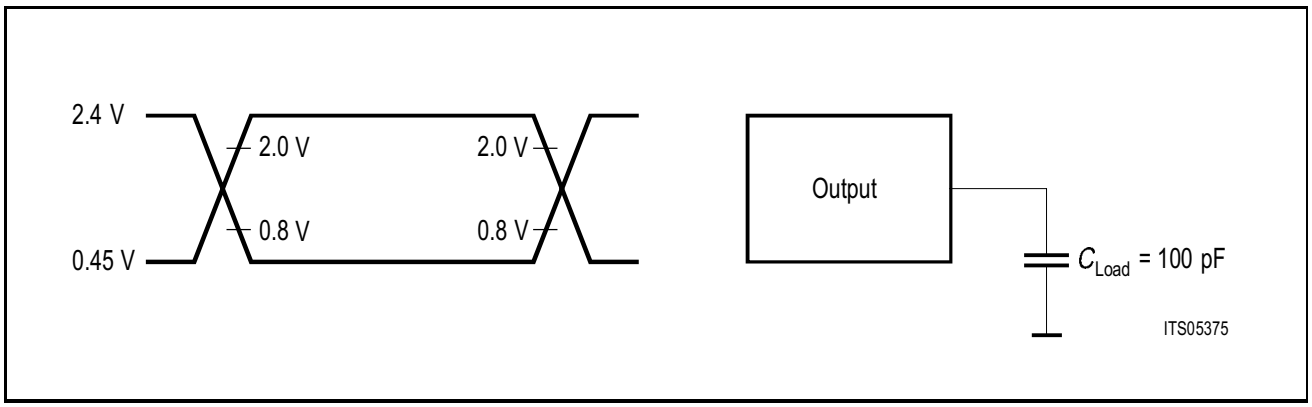


Figure 55
Input/Output Waveforms for AC-Tests

Serial Control Interface Timing

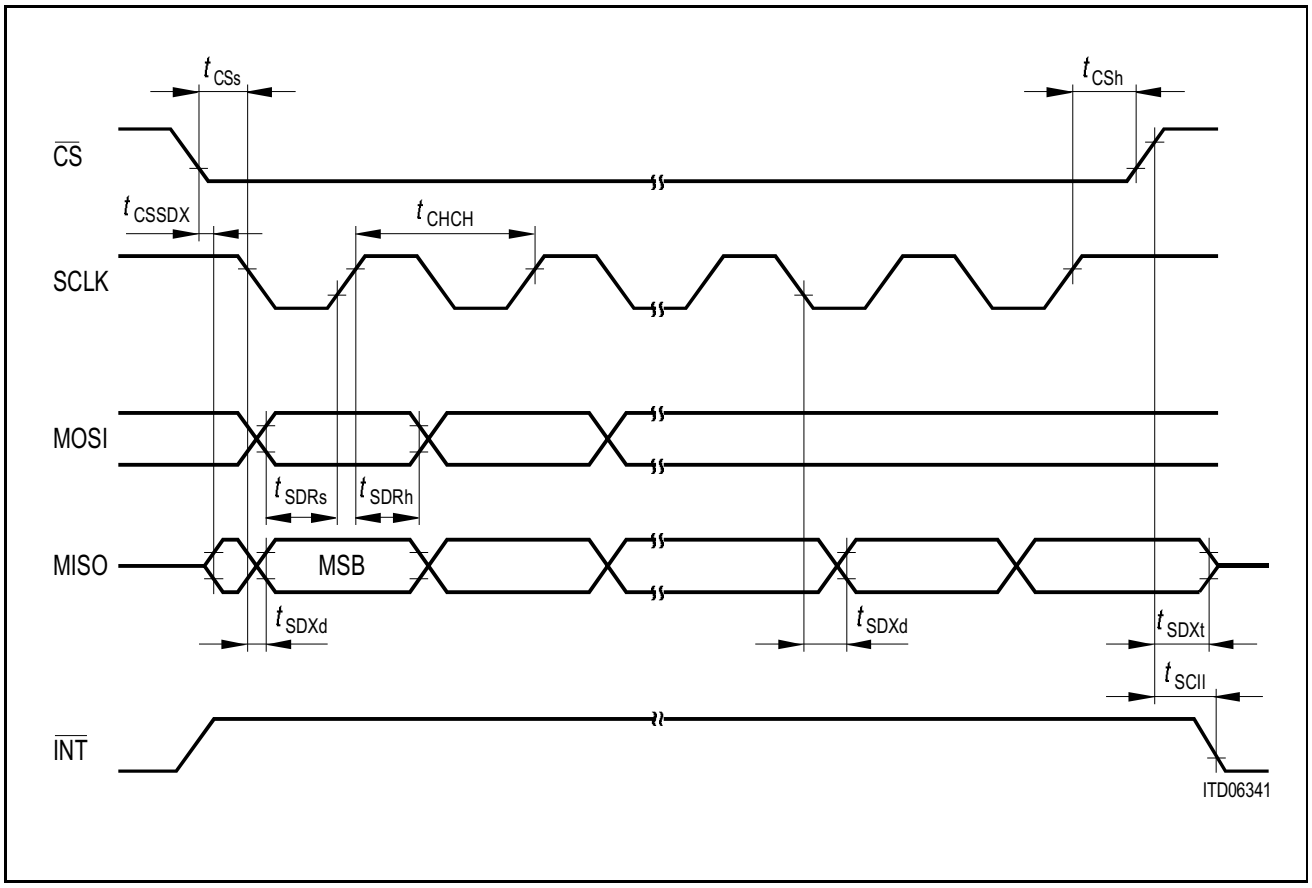


Figure 56
SCI-Switching Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
SCLK-frequency	t_{CHCH}	250		ns
Chip select setup time	t_{CSs}	10		ns
Chip select hold time	t_{CSh}	0		ns
MOSI-setup time	t_{SDRs}	50		ns
MOSI-hold time	t_{SDRh}	50		ns
MISO-data-out delay from $\overline{CS}$	t_{CSSDX}		150	ns
MISO-data-out delay	t_{SDXd}		150	ns
$\overline{CS}$ high to $\overline{INT}$ low	t_{CSIl}		150	ns
$\overline{CS}$ high to MISO-tristate	t_{SDXt}		30	ns

Note: The rise time on $\overline{INT}$ after $\overline{CS}$ becomes low depends on the external pull-up resistor.

IOM®-2 Bus Switching Characteristics

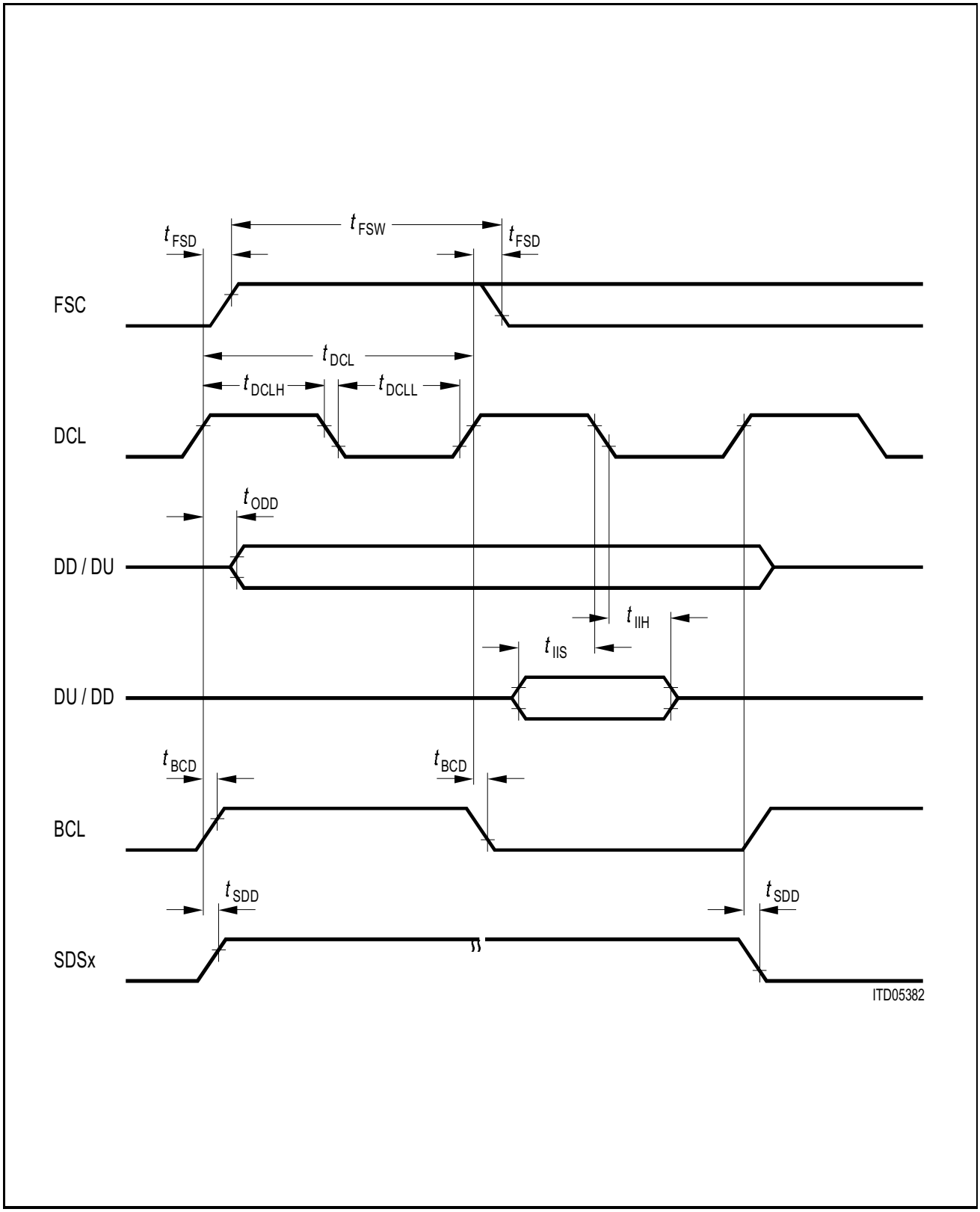


Figure 57
IOM®-2 TE-Mode (DCL, FSC output)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DCL-clock period (1.536 MHz)	t_{DCL}	585	651	717	ns
DCL-duty cycle		40	50	60	%
DCL-width high	t_{DCLH}	260	326	391	ns
DCL-width low	t_{DCLL}	260	326	391	ns
FSC-period	t_{FSC}		125		µs
FSC-setup delay	t_{FSD}	– 20		20	ns
FSC-width reduced FSC-length (1 DCL) nominal FSC-length (64 DCL)	t_{FSW}	585	651 41.6	717	ns µs
DU/DD-data-in setup time	t_{IIS}	50			ns
DU/DD-data-in hold time	t_{IIH}	50			ns
DU/DD-data-out delay	t_{ODD}			150	ns
Bit clock delay	t_{BCD}	– 20		20	ns
Strobe delay from DCL	t_{SDD}			120	ns

Note: Reduced FSC-length is output every eighth frame triggered by a CV in the received M-bit.

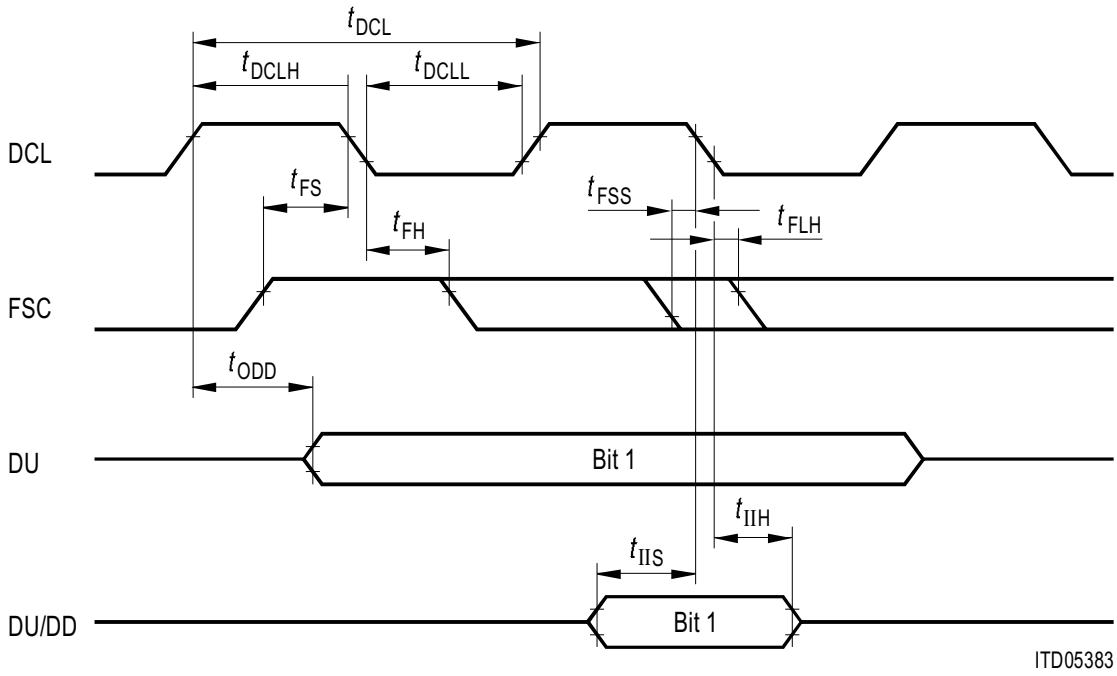


Figure 58
TR-, HDLC- Mode (DCL, FSC input)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DCL-clock period (1.536 MHz)	t_{DCL}	488	651	814	ns
DCL-duty cycle		30	50	70	%
DCL-width high	t_{DCLH}	163	326	489	ns
DCL-width low	t_{DCLL}	163	326	489	ns
FSC-period	t_{FSC}		125		µs
FSC-setup time	t_{Fs}	70			ns
FSC-hold time	t_{Fh}	40			ns
FSC-setup short[1)]	t_{FSS}	70			ns
FSC-hold long[2)]	t_{FLH}	40			ns
DU/DD-data-in setup time	t_{IIs}	50			ns
DU/DD-data-in hold time	t_{IIh}	50			ns
DU-data-out delay from DCL	t_{ODD}			150	ns

Notes: 1) Nominal FSC-length = 1 DCL-period (Trigger for M = CV-generation)
2) No trigger for M = CV-generation

MCLK-Timing

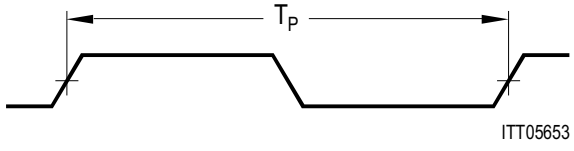


Figure 60
MCLK-Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Clock period 0.96 MHz	T_p		1042		ns
1.92 MHz	T_p		521		ns
3.84 MHz	T_p		260		ns
7.68 MHz	T_p		130		ns
Duty cycle			50		%

Reset Timings

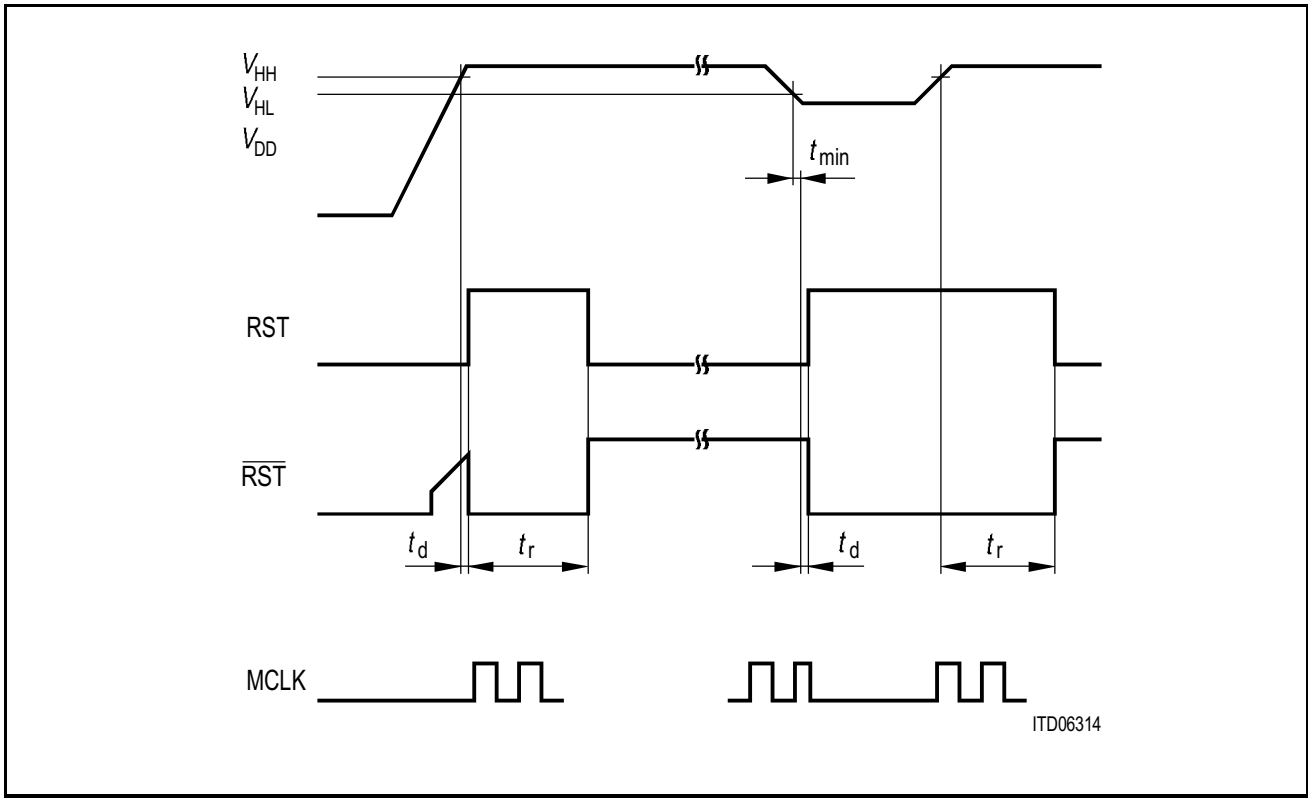


Figure 59
Undervoltage Detection

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Threshold value	V_{HL}	4.2	4.4	V
Hysteresis	$V_{HH} - V_{HL}$	50	230	ms
Minimum voltage drop	T_{min}		11	µs
Delay from V_{HH} crossing to reset active	T_d		1	µs

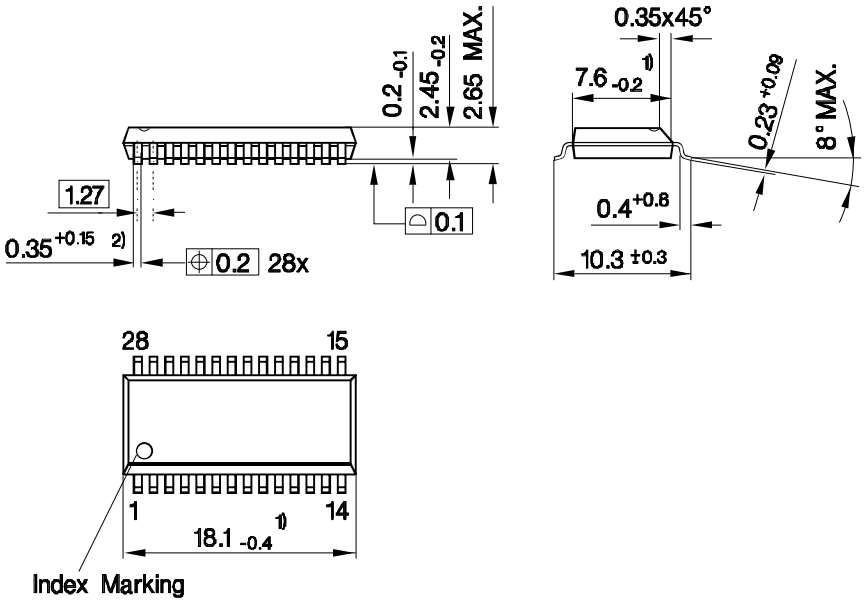
V_{HL} and ($V_{HH} - V_{HL}$) values are tested at room temperature.

Typical temperature drift is – 8 mV per + 10 °C temperature drift for V_{HL} and + 3 mV per + 10 °C for the hysteresis value.

Components are tested at 75 °C at which the absolute minimum V_{HL}-level is set to 4.14 V for pass condition.

6 Package Outlines

Plastic Package, P-DSO-28-1 (SMD)
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

GPS05123

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”
SMD = Surface Mounted Device

Dimensions in mm