256K Dynamic RAM Controller/Driver

SN74S409-2/DP8409A-2
SN74S409/DP8409A

Features/Benefits

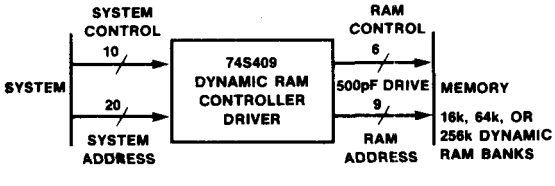
- All DRAM drive functions on one chip have on-chip high-capacitance load drivers (specified up to 88 DRAMs)
- Drives directly all 16K, 64K and 256K DRAMs; capable of addressing up to 1M words
- Propagation delays of 25 nsec typical at 500 pF load
- Supports READ, WRITE and READ-MODIFY-WRITE cycles
- Eight modes of operation support externally-controlled and automatic access and refresh, as well as special memory initialization access
- On-chip 9-bit refresh counter with selectable End-of-Count (127, 255 or 511)
- Direct replacement for National DP8409, DP8409A

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
SN74S409	48 N, D	Com
SN74S409-2	48 N, D	Com, Speed Option

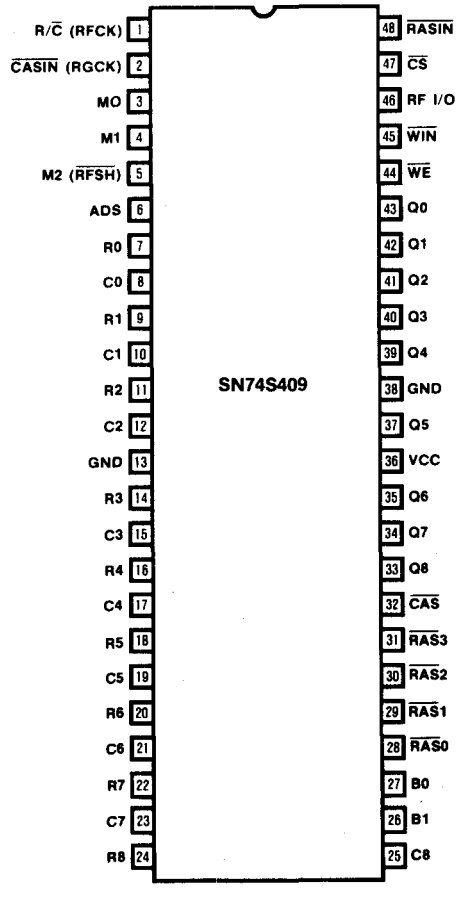
Operating Modes

0	Externally-controlled fresh
1	Auto refresh—forced
2	Automatic burst refresh
3a	All-$\overline{RAS}$ auto write
3b	Externally-controlled All-$\overline{RAS}$ write
4	Externally-controlled access
5	Auto access, slow t_{RAH}, hidden refresh
6	Auto access, fast t_{RAH}
7	Set end of count



Interface Between System and DRAM Banks

Pin Configuration



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Monolithic Memories

Block Diagram

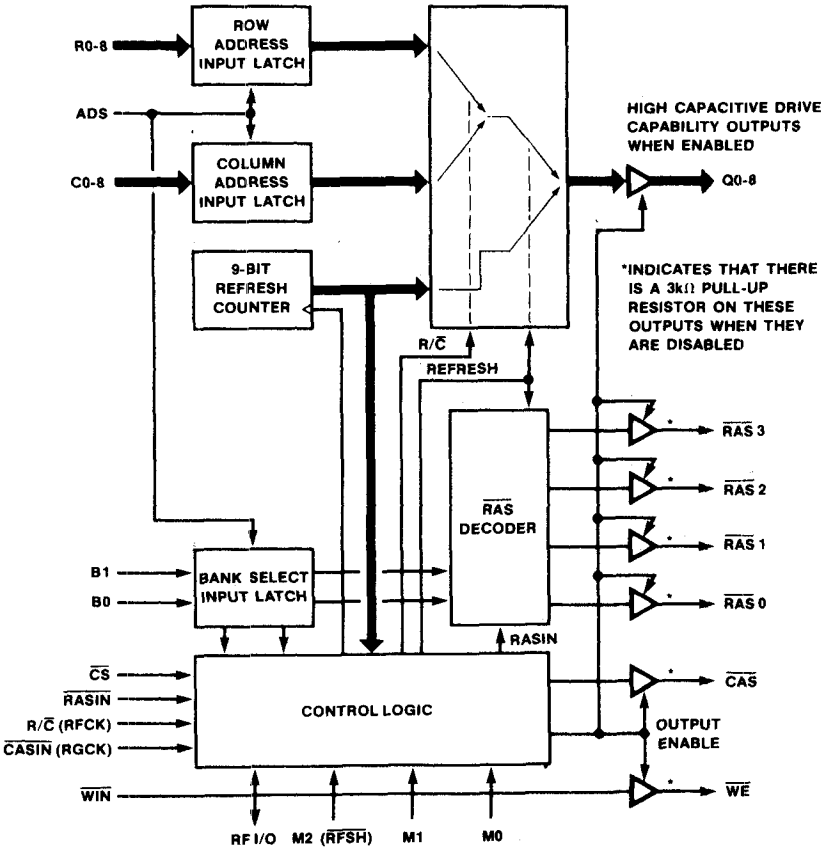

Figure 1. 74S409 Functional Block Diagram

Description

The 74S409 is a Multi-Mode Dynamic RAM Controller/Driver capable of directly driving up to 88 DRAMs. 20 address lines to the 74S409 allow it to address up to 1M words and it can drive 16K, 64K and 256K DRAMs. Since the 74S409 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, and saves board space.

The 74S409's 8 operating modes offer externally-controlled or on-chip automatic access and refresh. An on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.

The 74S409 is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control logic. The 74S409 timing parameters are specified when driving the typical load capitance of 88 DRAMs, including trace capacitance.

The 74S409 can drive up to 4 banks of DRAMs, with each bank comprised of 16Ks, 64Ks or 256Ks. Control signal outputs $\overline{CAS}$ and $\overline{WE}$ are provided with the same driving capability. Each $\overline{RAS}$ output drives one bank of DRAMs so that the four $\overline{RAS}$ outputs are used to select the banks, while $\overline{CAS}$, $\overline{WE}$ and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the respective data outputs in three-state. Only the bank with its associated $\overline{RAS}$ low will be written to or read from, except in mode 3 where all $\overline{RAS}$ signals go low to allow fast memory initialization.

Pin Definitions

V_{CC} GND, GND—V_{CC} = 5V ± 5%. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution is a 1-μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

R0-R8: Row Address Inputs.

C0-C8: Column Address Inputs.

B0, B1: Bank Select Inputs—Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes low, in modes 4-6. In mode 7 B0, B1 are used to define End-of-Count (see table 3), and select mode 3a or 3b.

Q0-Q8: Multiplexed Address Outputs—Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.

$\overline{RASIN}$: Row Address Strobe Input—Enables selected $\overline{RAS}_n$ output when M2 ($\overline{RFSH}$) is high (modes 4-6), and all $\overline{RAS}_n$ outputs in modes 0 and 3. $\overline{RASIN}$ input is disabled in modes 1 and 2.

R/$\overline{C}$ (RFCK)—In Auto-Refresh Mode this pin is the external Refresh Clock Input: one refresh cycle has to be performed each clock period. In all other modes it is Row/$\overline{Column}$ Select Input, selecting either the row or column address input latch onto the output bus.

$\overline{CASIN}$ (RGCK)—In modes 1, 2 and 3a, this pin is the $\overline{RAS}$ Generator Clock input. In all other modes it is $\overline{CASIN}$ (Column Address Strobe Input), which inhibits $\overline{CAS}$ output when high in Modes 3b and 4. In Mode 6 it can be used to prolong $\overline{CAS}$ output.

ADS: Address (Latch) Strobe Input—Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; latches on High-to-Low transition.

$\overline{CS}$: Chip Select Input—three-state's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in one of the Refresh Modes). Enables all outputs when low.

M0, M1, M2 ($\overline{RFSH}$): Mode Control Inputs—These 3 control pins determine the 8 major modes of operation of the 74S409 as depicted in Table 2.

RF I/O $\overline{RFRQ}$ — This I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low in Modes 0, 2 and 3a when the End-of-Count output is at 127, 255, or 511 (see Table 3). In Auto-Refresh Mode (mode 5) it is the $\overline{Refresh}$ $\overline{Request}$ ($\overline{RFRQ}$) output.

BANK SELECT (STROBED BY ADS)		ENABLED $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

Table 1. Memory Bank Decode

$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output—Buffered output from $\overline{WIN}$.

$\overline{CAS}$: Column Address Strobe Output—In Modes 3a, 5, and 6, $\overline{CAS}$ transitions low following valid column address. In Modes 3b and 4, it goes low after R/$\overline{C}$ goes low, or follows $\overline{CASIN}$ going low if R/$\overline{C}$ is already low. $\overline{CAS}$ is high during refresh.

$\overline{RAS}$ 0-3: Row Address Strobe Outputs—When M2($\overline{RFSH}$) is high (modes 4-6), the selected row address strobe output (decoded from signals B0, B1) follows the $\overline{RASIN}$ input. When M2 ($\overline{RFSH}$) is low (modes 0-3) all $\overline{RAS}_n$ outputs go low together following $\overline{RASIN}$ going low in modes 0 and 3 and automatically in modes 1 and 2.

Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter.

The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid address until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the address is still valid.

In normal memory-access operation, $\overline{RASIN}$ and R/$\overline{C}$ are initially high. When the address inputs are enabled into the address latches (modes 3-6) the row addresses appear on the Q outputs. The Address Strobe also inputs the bank-select address, (B0 and B1). If $\overline{CS}$ is low, all outputs are enabled. When $\overline{CS}$ goes high, the address outputs go three-state and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S409s for multi-addressing. All outputs go active about 50ns after the chip is selected again. If $\overline{CS}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

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Drive Capability

The 74S409 has timing parameters that are specified with up to 600pF loads for $\overline{CAS}$ and $\overline{WE}$, 500pF loads for Q_0-Q_8, and 150pF loads for $\overline{RAS}_n$ outputs. In a typical memory system this is equivalent to about 88 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 14. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

74S409 Driving Any 16K, 64K or 256K DRAMs

The 74S409 can drive any 16K, 64K, or 256K DRAMs. The on-chip 9-bit counter with selectable End-of-Count can support refresh of 128, 256 and 512 rows, while the 9 address and 4 $\overline{RAS}_n$ outputs can address 4 banks of 16K, 64K or 256K DRAMs.

Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

Power-Up Initialize

When V_{CC} is first applied to the 74S409, an internal pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to three-state. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

74S409 Functional Modes Description

The 74S409 operates in 8 different functional modes selected by signals M_0,M_1,M_2. Mode 3 splits further to modes 3a and 3b determined by signals B_0,B_1 in mode 7.

Mode 0 and mode 1 are generally used as Refresh modes for mode 4 and mode 5 respectively, and therefore will be described as mode-pairs 0,4 and 1,5.

Mode 6 is a fast access made for very fast DRAMs and mode 7 is used only to determine choice of mode 3a or 3b and for setting End-of-Count for the refresh modes.

MODE	($\overline{RFSH}$) M2	M1	M0	MODE OF OPERATION	CONDITIONS
0	0	0	0	Externally-controlled refresh	RF I/O = $\overline{EOC}$
1	0	0	1	Auto refresh – forced	RF I/O = Refresh request ($\overline{RFRQ}$)
2	0	1	0	Automatic burst refresh	RF I/O = $\overline{EOC}$
3a*	0	1	1	All-$\overline{RAS}$ auto write	RF I/O = $\overline{EOC}$; all $\overline{RAS}$ active
3b*	0	1	1	Externally-controlled All-$\overline{RAS}$ write	All-$\overline{RAS}$ active
4	1	0	0	Externally-controlled access	Active $\overline{RAS}$ defined by Table 2
5	1	0	1	Auto access, slow t_{RAH}, hidden refresh	Active $\overline{RAS}$ defined by Table 2
6	1	1	0	Auto access, fast t_{RAH}	Active $\overline{RAS}$ defined by Table 2
7	1	1	1	Set end of count; determines mode 3a or 3b	See Table 3 for Mode 7

*Mode 3a is selected by setting B_0,B_1 to 01, 00, or 10 in mode 7.
*Mode 3b is selected by setting B_1,B_0 to 11 in mode 7.

Table 2. 74S409 Mode Select Options

Mode 0 — Externally-Controlled Refresh
Mode 4 — Externally-Controlled Access

Modes 0 and 4 facilitate external control of all timing parameters associated with the DRAMs. These modes are independent modes of operation though generally used together in the same application as shown in Figure 2.

Mode 0—Externally-Controlled Refresh

In this mode the input address latches are disabled from the address outputs and the refresh counter is enabled. All $\overline{RAS}$ outputs go low following $\overline{RASIN}$ and refresh the enabled row in all four banks. $\overline{CASIN}$ and R/$\overline{C}$ inputs are not used and $\overline{CAS}$ is inhibited. The refresh counter increments when either $\overline{RASIN}$ or M2 ($\overline{RFSH}$) switch high while the other is still low.

RF I/O goes low when the count equals End-of-Count (as set in mode 7), and $\overline{RASIN}$ is low. The 9-bit counter will always roll-over to zero at 512, regardless of End-of-Count. However, the counter can be reset at any time by driving RF I/O low through an external open-collector.

During refresh, $\overline{RASIN}$ and M2 ($\overline{RFSH}$) can transition low simultaneously because the refresh counter becomes valid on the output bus t_{RFLCT} after $\overline{RFSH}$ goes low, which is a shorter time than t_{RFPDL}. This means the counter address is valid on the Q outputs before $\overline{RAS}$ occurs on all $\overline{RAS}$ outputs, strobing the counter address into that row of all the DRAMs (see Figure 2.). To perform externally-controlled burst refresh, $\overline{RFSH}$ initially can again have the same edge as $\overline{RASIN}$, but then maintains a low state, since $\overline{RASIN}$ going low-to-high increments the counter (performing the burst refresh).

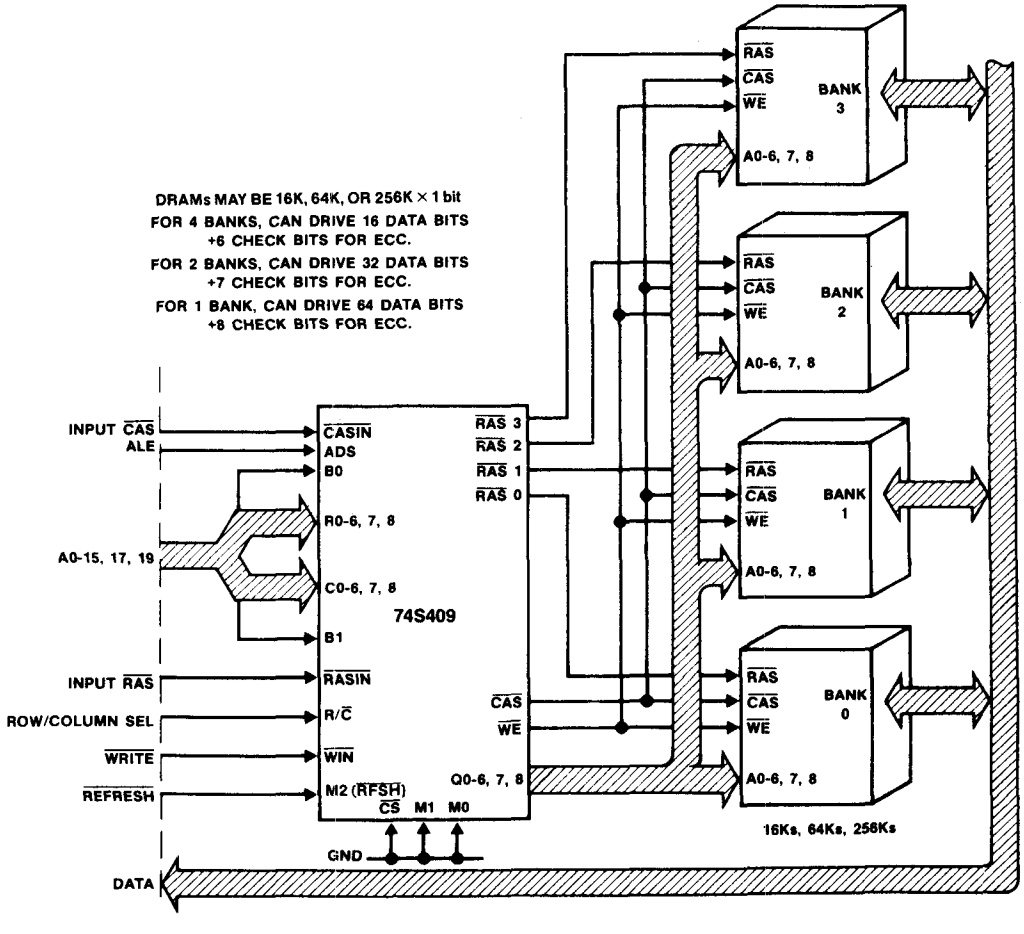
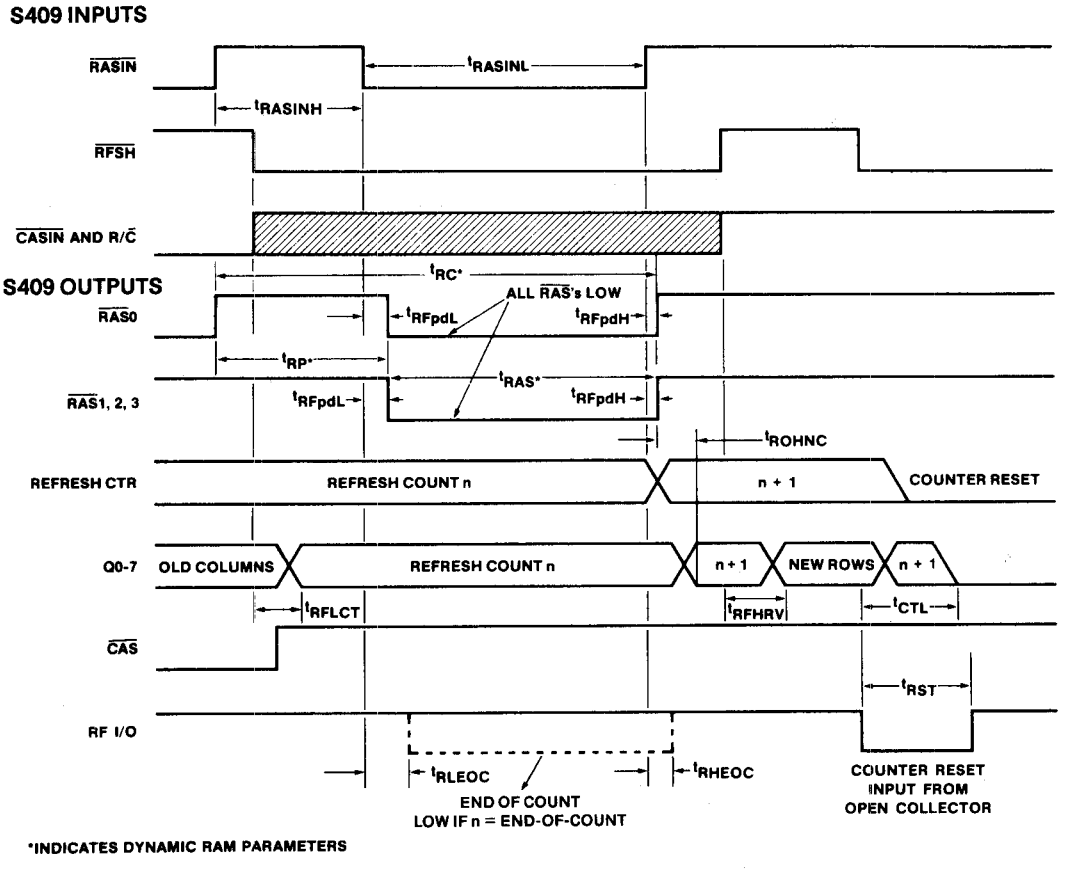


Figure 2. Typical Application of 74S409 Using Externally-Controlled Access and Refresh in Modes 0 and 4



*INDICATES DYNAMIC RAM PARAMETERS

Figure 3. External Control Refresh Cycle (Mode 0)

Mode 4 — Externally-Controlled Access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. Figures 4 and 5 show the timing for read and write cycles.

Output Address Selection

In this mode $\overline{CS}$ has to be low at least 50 nsec before the outputs will be valid. With R/$\overline{C}$ high, the row address latch contents are transfered to the multiplexed address bus output Q0-Q8. $\overline{RASIN}$ can go low after the row addresses have been set up on Q0-Q8, and enables one $\overline{RAS}$ output selected by signals B0, B1 to strobe the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go low so that about 40 nsec later, the column address appears on the Q output.

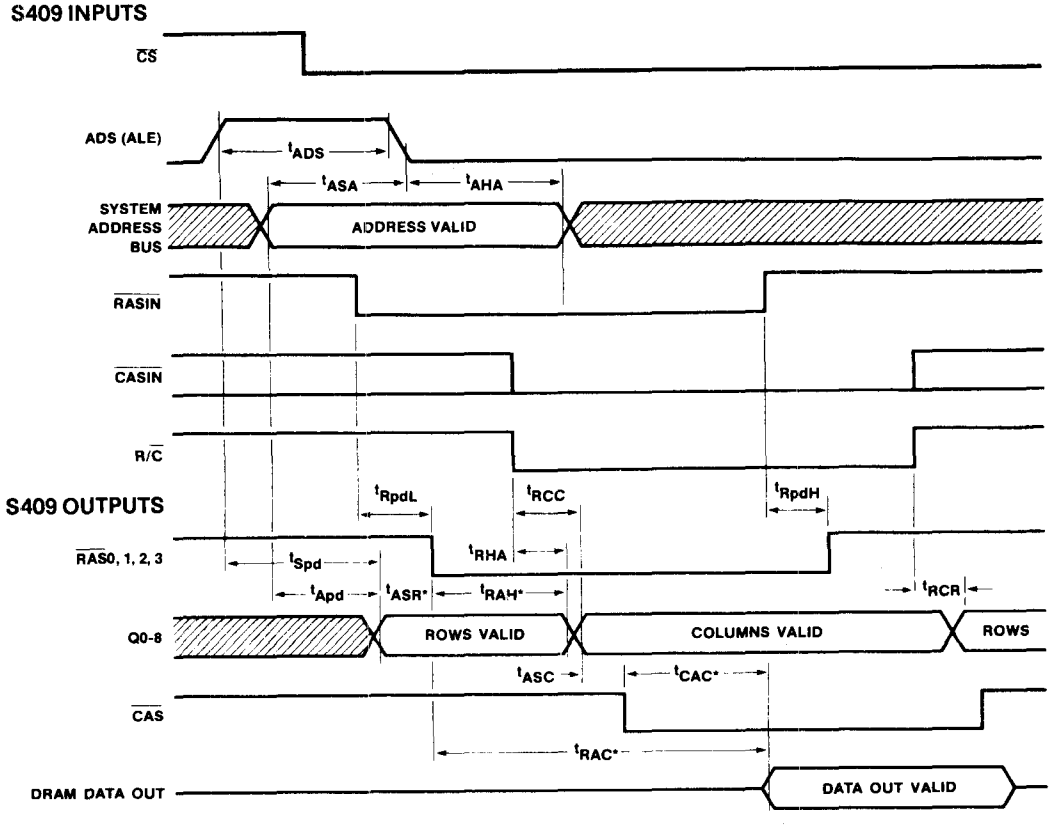


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Figure 4. Read Cycle Timing (Mode 4)

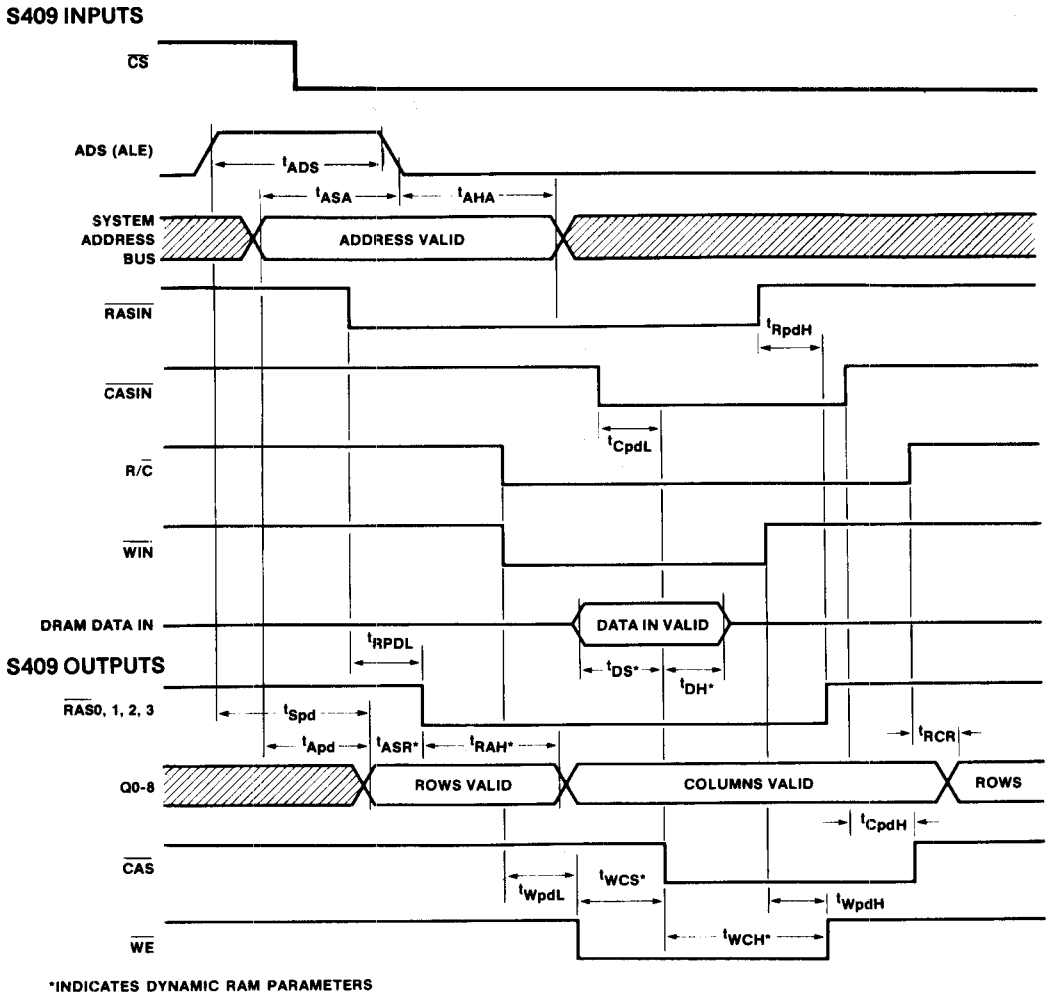

Figure 5. Write Cycle Timing (Mode 4)

Automatic $\overline{CAS}$ Generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs $\overline{CASIN}$ or R/$\overline{C}$. If $\overline{CASIN}$ is high, then R/$\overline{C}$ going low switches the address output drivers from rows to columns. $\overline{CASIN}$ then going low causes $\overline{CAS}$ to go low approximately 40 ns later, allowing $\overline{CAS}$ to occur at a predictable time (see Figure 5). For maximum system speed, $\overline{CASIN}$ can be kept low, since $\overline{CAS}$ will automatically occur approximately 60 ns after R/$\overline{C}$ goes low (see Figure 4). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of 0 ns or −10 ns. In other words, a t_{ASC} greater than 0 ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

For faster access time, R/$\overline{C}$ can go low a time delay ($t_{RPDL} + t_{RAH} - t_{RHA}$) after $\overline{RASIN}$ goes low, where t_{RAH} is the Row-Address hold-time of the DRAM, and $\overline{CASIN}$ can go low $t_{RCC} - t_{CPOL} + t_{ASC}$ (min.) after R/$\overline{C}$ goes low (see t_{DiF1}, t_{DiF2} switching characteristics).

Mode 1 – Automatic Forced Refresh Mode 5 – Automatic Access with Hidden Refresh

Mode 1 and Mode 5 are generally used together incorporating the advantages of the "hidden refresh" performed in mode 5 with the possibiity to force a refresh by changing to mode 1. An advantage of the Automatic Access over the Externally-Controlled Access is the reduced memory access time, due to the fact that the output control signals are derived internally from one input signal ($\overline{RASIN}$).

Hidden and Forced Refresh

Hidden Refresh is a term describing memory refresh performed when the system does not access the portion of memory controlled by the 74S409 ($\overline{CS}$ = 1). A hidden refresh will occur once per Refresh Clock (RFCK) cycle provided $\overline{CS}$ went high and $\overline{RASIN}$ went low. If no hidden refresh occurred while RFCK was high, the RF I/O ($\overline{RFRQ}$) goes low immediately after RFCK goes low, indicating to the system when a forced refresh is required. The system must allow a forced refresh to take place while RFCK is low by driving M2 ($\overline{RFSH}$) low, thereby changing mode of operation to Mode 1.

The Refresh Request on RF I/O ($\overline{RFRQ}$) is terminated as soon as $\overline{RAS}$ goes low, indicating to the system that the foced refresh has been done. The system should then drive M2 ($\overline{RFSH}$) high, changing the mode of operation back to Mode 5 (see Figure 6).

Mode 1 – Automatic Forced Refresh

In Mode 1, the R/$\overline{C}$ (RFCK) pin functions as RFCK (refresh cycle clock) instead of R/$\overline{C}$, and $\overline{CAS}$ remains high. If RFCK is kept permanently high then whenever M2 ($\overline{RFSH}$) goes low, an externally-controlled refresh will occur and all $\overline{RAS}$ outputs will follow $\overline{RASIN}$, strobing the refresh counter contents to the DRAMs. The RF I/O pin will always output high, but can be set low externally through an open-collector driver, to reset the refresh counter.

If RFCK is an input clock, one and only one refresh cycle must take place every RFCK cycle. If a hidden refresh does not occur while RFCK is high, in Mode 5, then RF I/O ($\overline{Refresh\ Request}$) goes low immediately after RFCK goes low, indicating to the system that a forced refresh is required. The system must allow a forced refresh to take place while RFCK is low The Refresh Request signal on RF I/O may be connected to a Hold or Bus Request input to the system. The system acknowledges the Hold or Bus Request when ready, and outputs Hold Acknowledge or Bus Request Acknowledge. If this is connected to the M2 ($\overline{RFSH}$) pin, a forced-refresh cycle will be initiated by the S409, and $\overline{RAS}$ will be internally generated on all four $\overline{RAS}$ outputs, strobing the refresh counter contents on the address ouputs into all the DRAMs. An external $\overline{RAS}$ Generator Clock (RGCK) is requred for this function. It is fed to the $\overline{CASIN}$ (RGCK) pin, and may be up to 10 MHz. Whenever M2 goes low (inducing a forced refresh), $\overline{RAS}$ remains high for one to two periods of RGCK, depending on when M2 goes low relative to the high-to-low triggering edge of RGCK; $\overline{RAS}$ then goes low for two periods, performing a refresh on all banks. In order to obtain the minimum delay from M2 going low to $\overline{RAS}$ going low, M2 should go low t_{RFSRG} before the next falling edge of RGCK. The Refresh Request on RF I/O is terminated as $\overline{RAS}$ begins, so that by the time the system has acknowledged the removal of the request and disabled its Acknowledge, (i.e., M2 goes high), Refresh $\overline{RAS}$ will have ended, and normal operations can begin again in the Automatic Access mode (Mode 5). If it is desired that Refresh $\overline{RAS}$ end in less than 2 periods of RGCK from the time $\overline{RAS}$ went low, then M2 may go high earlier than t_{FRQH} after RF I/O goes high and $\overline{RAS}$ will go high t_{RFRH} after M2.

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Mode 5 – Automatic Access with Hidden Refresh

In this mode all address outputs, $\overline{RAS}$ and $\overline{CAS}$ are initiated from $\overline{RASIN}$ making the DRAM access appear similar to static RAM access. The hidden refresh feature enables DRAM refresh accomplished with no time-loss to the system.

Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S409. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S409 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASR} before ADS went low (see Figure 7).

Next, the row address is disabled t_{RAH} after $\overline{RAS}$ goes low (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and (t_{ASC} later,) $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

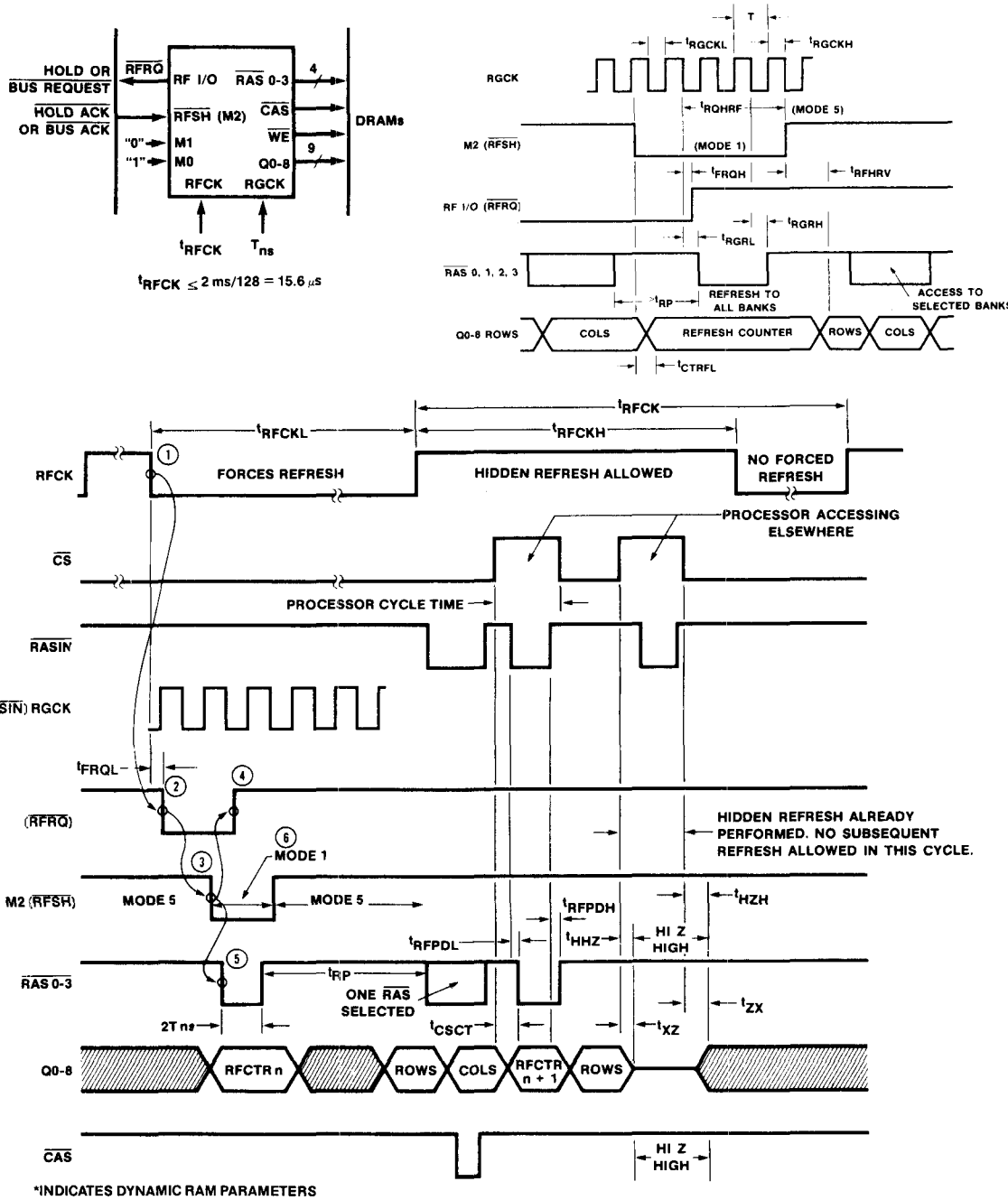
Refreshing

In this mode R/$\overline{C}$ (RFCK) functions as Refresh Clock and $\overline{CASIN}$ (RGCK) functions as $\overline{RAS}$ Generator Clock.

One refresh cycle must occur during each refresh clock period, and then the refresh address must be incremented before the next refresh cycle. As long as 128 rows are refreshed every 2 ms (one row every 16 μs), all 16K and 64K DRAMs will be correctly refreshed. The cycle time of RFCK must, therefore, be less than 16 μs. RFCK going high sets an internal refresh-request flipflop. First the 74S409 will attempt to perform a hidden refresh so that the system thruput will not be affected. If, during the time RFCK is high, $\overline{CS}$ on the 74S409 goes high and $\overline{RASIN}$ occurs, a hidden refresh will occur. In this case, $\overline{RASIN}$ should be considered a common read/write strobe. In other words, if the processor is accessing elsewhere (other than the DRAMs) while RFCK is high, the 74S409 will perform a refresh. The refresh counter is enabled to the address outputs whenever $\overline{CS}$ goes high with RFCK high, and all $\overline{RAS}$ outputs follow $\overline{RASIN}$. If a hidden refresh is taking place as RFCK goes low, the refresh continues. At the start of the hidden refresh, the refresh-request flipflop is reset so on further refresh can occur until the next RFCK period starts with the positive-going edge of RFCK (see Figure 6). $\overline{RASIN}$ should go low at least 20 ns before RFCK goes low, to ensure occurrence of the hidden refresh.

To determine the probability of a hidden refresh occurring, goes low, (and the internal-request flipflop has not been for 8μs, then the system has 20 chances to not select the 74S409. If during this time a hidden refresh did not occur, then the 74S409 forces a refresh while RFCK is low, but the system chooses when the refresh takes place. After RFCK goes low, (and the internal-request flip-flop has not been reset), RF I/O goes low indicating that a refresh is requested to the system. Only when the system acknowledges this request by setting M2 ($\overline{RFSH}$) low does the 74S409 initiate a forced refresh (which is performed automatically). Refer to Mode 1, and Figure 6. The internal refresh request flipflop is then reset.

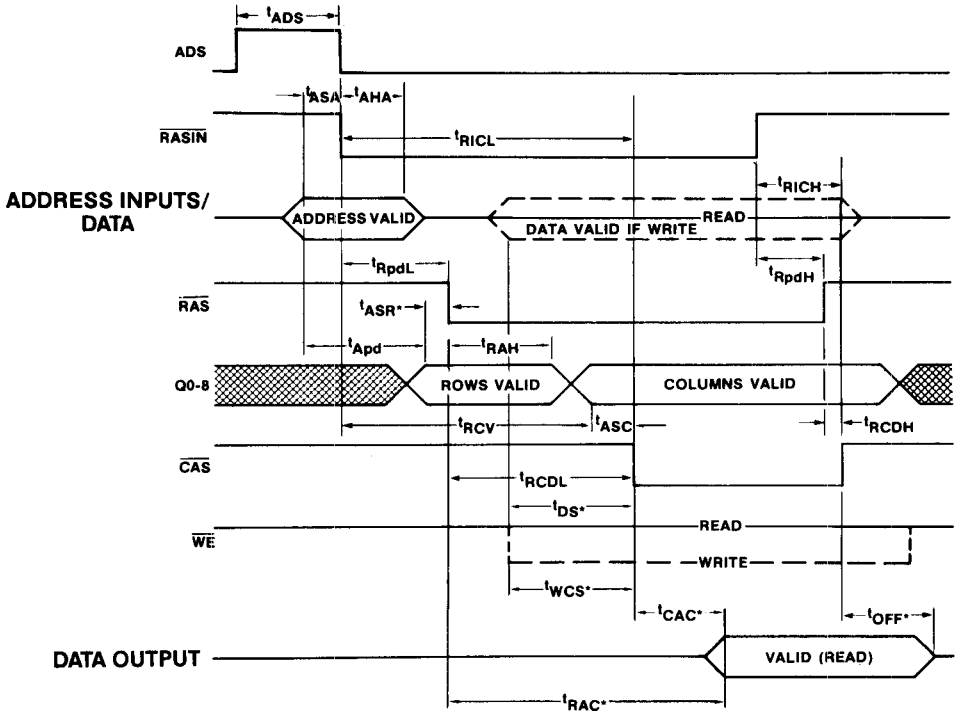
Figure 6 illustrates the refresh alternatives in Mode 5. If a hidden refresh has occurred and $\overline{CS}$ again goes high before RFCK goes low, the chip is deselected. All the control signals go high-impedance high (logic "1") and the address outputs go three-state until $\overline{CS}$ again goes low. This mode (combined with Mode 1) allows very fast access, and automatic refreshing (possibly not even slowing down the system), with no extra ICs. Careful system design can, and should, provide a higher probability of hidden refresh occurring. The duty cycle of RFCK need not be 50 percent; in fact, the low-time should be designed to be a minimum. This is determined by the worst-case time (required by the system) to respond to the 74S409's forced-refresh request.



*INDICATES DYNAMIC RAM PARAMETERS

1. RFCK GOES LOW
2. RFRQ GOES LOW IN NO HIDDEN REFRESH OCCURRED WHILE RFCK WAS HIGH
3. M2 (RFSH) DRIVEN LOW EXTERNALLY
4. REFRESH REQUEST RELEASED
5. RAS 0-3 GO LOW TO PERFORM REFRESH
6. M2 (RFSH) RELEASED

Figure 6. Hidden Refreshing (Mode 5) and Forced Refreshing (Mode 1) Timing



*INDICATES DYNAMIC RAM PARAMETERS

Figure 7. Mode 5 Timing

Mode 2—Automatic Burst Refresh

This mode is normally used before and/or after a DMA operation to ensure that all rows remain refreshed, provided the DMA transfer takes less than 2 ms (see Figure 8). When the 74S409 enters this mode, $\overline{CASIN}$ (RGCK) becomes the $\overline{RAS}$ Generator Clock (RGCK), and $\overline{RASIN}$ is disabled. $\overline{CAS}$ remains high, and RF I/O goes low when the refresh counter has reached the selected End-of-Count and the last $\overline{RAS}$ has ended. RF I/O then remains low until the Auto-Burst Refresh mode is terminated. RF I/O can therefore be used as an interrupt to indicate the End-of-Burst condition.

The signal on all four $\overline{RAS}$ outputs is just a divide-by-four of RGCK; in other words, if RGCK has a 100 ns period, $\overline{RAS}$ is high and low for 200 ns each cycle. The refresh counter increments at the end of each $\overline{RAS}$, starting from the count it contained when the mode was entered. If this was zero then for a RGCK with a 100 ns period with End-of Count set to 127, RF I/O will go low after 128 x 0.4μs, or 51.2μs. During this time, the system may be performing operations that do not involve DRAM. If all rows need to be burst refreshed, the refresh counter may be cleared by setting RF I/O low externally before the burst begins.

Burst-mode refreshing is also useful when powering down systems for long periods of time, but with data retention still required while the DRAMs are in standby. To maintain valid refreshing, power can be applied to the 74S409 (set to Mode 2), causing it to perform a complete burst refresh. When end-of-bust occurs (after 26 μs), power can then be removed from the 74S409 for 2 ms, consuming an average power of 1.3% of normal operating power. No control signal glitches occur when switching power to the 74S409.

Mode 3a—All-$\overline{RAS}$ Automatic Write

Mode 3a is useful at system initialization, when the memory is being cleared (i.e., with all-zeroes in the data field and the corresponding check bits for error detection and correction). This requires writing the same data to each location of memory (every row of each column of each bank). All $\overline{RAS}$ outputs are activated, as in refresh, and so are $\overline{CAS}$ and $\overline{WE}$. To write to all four banks simultaneously, every row is strobed in each column, in sequence, until data has been written to all locations. The refresh counter is used to address the rows, and $\overline{RAS}$ is low for two RGCK cycles and high for two cycles.

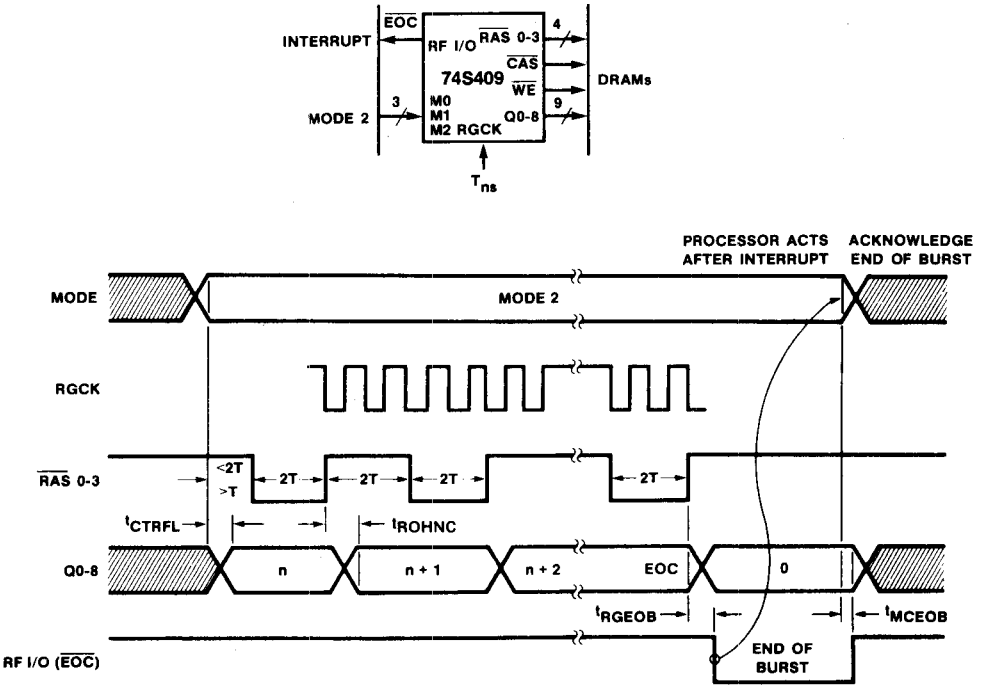
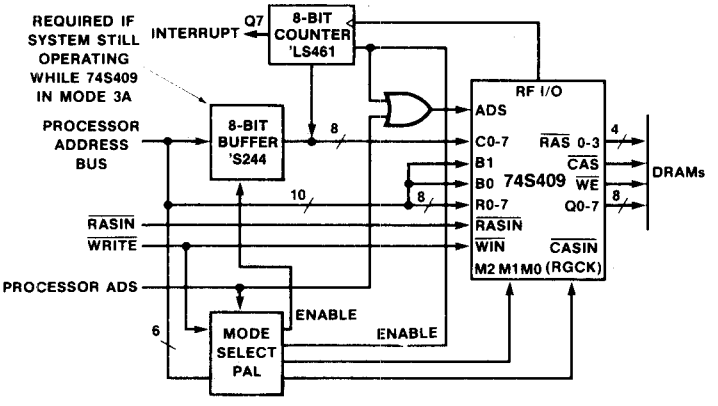


Figure 8. Auto-Burst Mode, Mode 2

To select this mode, B1 and B0 must have previously been set to 00, 01, or 10 in Mode 7, depending on the DRAM size. For example, for 16K DRAMs, B1 and B0 are 00. For 64K DRAMs, B1 and B0 are 01.

In this mode, R/$\overline{C}$ is disabled, $\overline{WE}$ is permanently enabled low, and $\overline{CASIN}$ (RGCK) becomes RGCK. RF I/O goes low whenever the refresh counter is 127, 255, or 511 (as set by End-of-Count in Mode 7), and the $\overline{RAS}$ outputs are active.



74S409 Extra Circuitry Required for All-$\overline{RAS}$ Auto Write Mode, Mode 3a

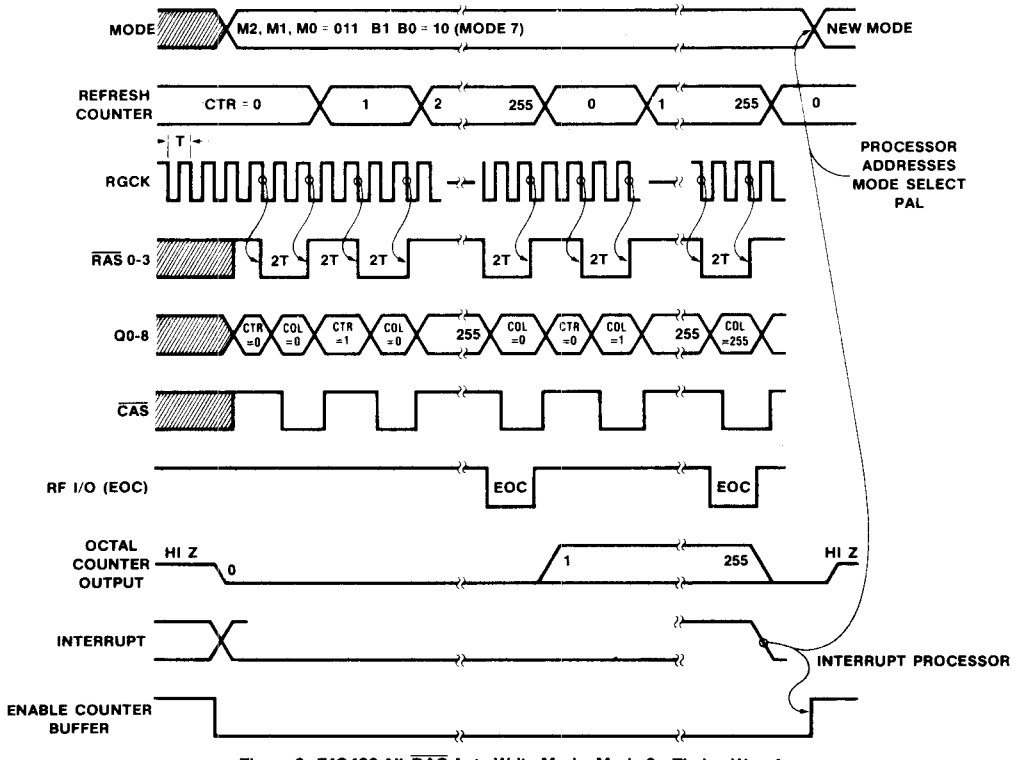


Figure 9. 74S409 All-$\overline{RAS}$ Auto Write Mode, Mode 3a, Timing Waveform

Mode 3b — Externally-Controlled All-$\overline{RAS}$ Write

To select this mode, B1 and B0 must first have been set to 11 in Mode 7. This mode is useful at system initialization, but under processor control. The memory address is provided by the processor, which also performs the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally-Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74S409 for the next write cycle. This method is slower than Mode 3a, since the processor must perform the incrementing and accessing. Thus the processor is occupied during RAM initialization, and is not free for other initialization operations. However, initialization sequence timing is under system control, which may provide some system advantage.

Mode 4 — Externally-Controlled Access

Mode 4 is described in with mode 0 in section "Mode 0 and Mode 4."

Mode 5 — Automatic Access with Hidden Refresh

See description of mode 0 and mode 5.

Mode 6 — Fast Automatic Access

The Fast Automatic Access mode can only be used with fast DRAMs which have t_{RAH} of 10 nsec-15nsec. The typical $\overline{RASIN}$ to $\overline{CAS}$ delay is 105nsec. In this mode $\overline{CAS}$ can be extended after $\overline{RAS}$ goes high to extend the data output valid time. This feature is useful in applications with short cycles where $\overline{RAS}$ has to be terminated as soon as possible to meet the precharge (t_{RP}) requirements of the DRAM.

Mode 6 timing is illustrated in Figures 10 and 11. Provided that the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S409. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The 74S409 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 10).

Next, the row address is disabled t_{RAH} after $\overline{RAS}$ goes low (20 ns minimum); the column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns): to rows valid (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

In this mode, the R/$\overline{C}$ (RFCK) pin is not used, but $\overline{CASIN}$ (RGCK) is used as $\overline{CASIN}$ to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to Figure 11.

Mode 7 — Set End-of-Count (3a, 3b select)

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same $\overline{EOC}$ is 127; with B1 = 0 and B0 = 1, $\overline{EOC}$ is 255; and with B1 = 1 and B0 = 0, $\overline{EOC}$ is 511. This selected value of $\overline{EOC}$ will be used until the next Mode 7 selection. At power-up the $\overline{EOC}$ is automatically set to 127 (B1 and B0 set to 11).

When B_1,B_2 are set to 11 in mode 7, mode 3b will be selected if mode 3 is selected (M_2, M_1, M_0 = 0, 1, 1). If B_1,B_2 is set to 00, 01 or 10 then mode 3a will be selected.

BANK SELECT (STROBED BY ADS)		END OF COUNT SELECTED
B1	B0	
0	0	127
0	1	255
1	0	511
1	1	127

Table 3. Mode 7

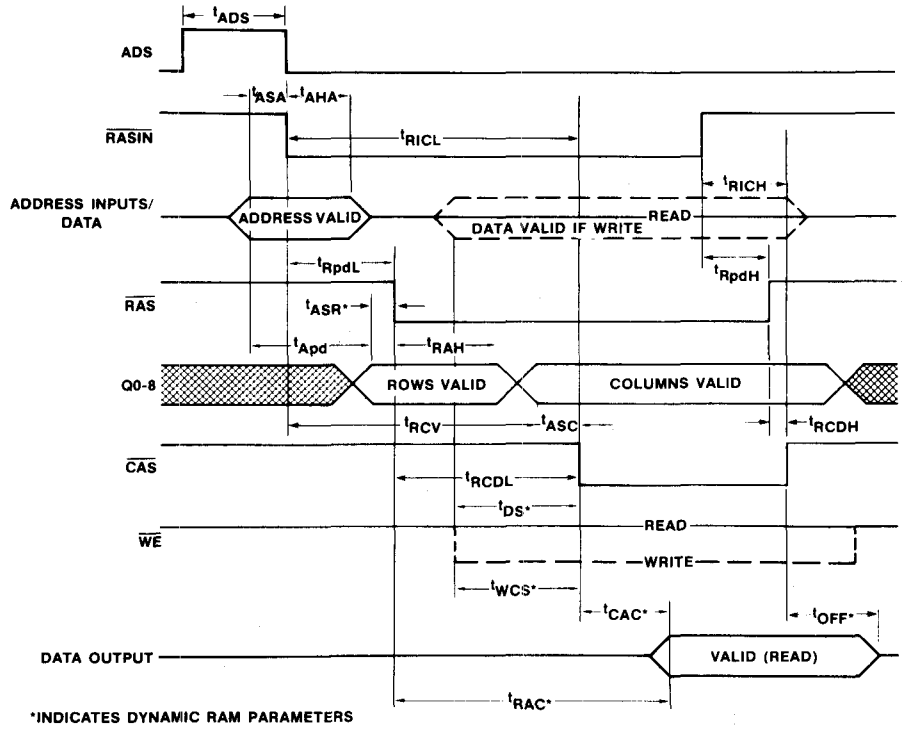


Figure 10. Mode 6 Timing ($\overline{\text{CASIN}}$ High)

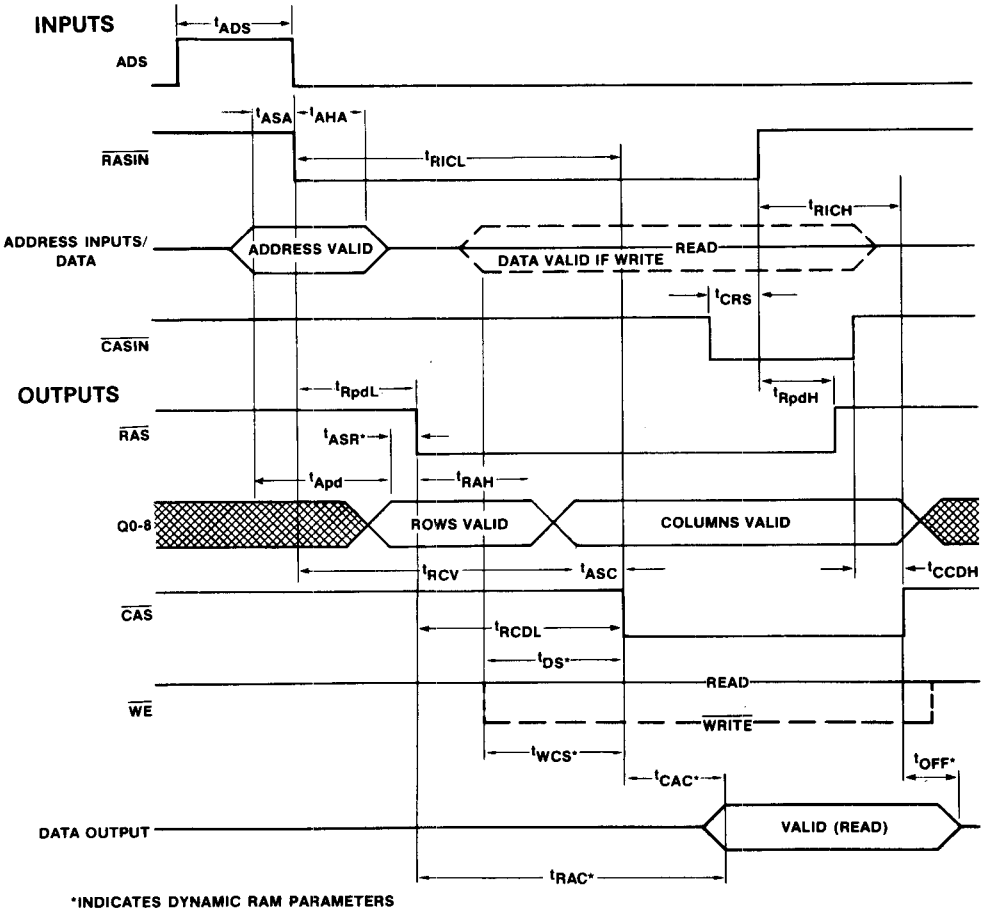


Figure 11. Mode 6 Timing, Extended $\overline{CAS}$

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SN74S409/-2 Specifications:

Absolute Maximum Ratings (Note 1)

Supply voltage V_{CC} ..... -0.5 V to 7.0 V
Storage temperature range ..... -65° to +150°C
Input voltage ..... -1.5 V to 5.5 V
Output current ..... 150 mA
Lead temperature (soldering, 10 seconds) ..... 300°C

NOTE 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	4.75		5.25	V
T_A	Operating free-air temperature		0		75	0		75	°C
t_{ASA}	Address setup time to ADS	Figures 4, 5, 7, 10, 11	15			15			ns
t_{AHA}	Address hold time from ADS	Figures 4, 5, 7, 10, 11	15			15			ns
t_{ADS}	Address strobe pulse width	Figures 4, 5, 7, 10, 11	30			30			ns
$t_{RASINL,H}$	Pulse width of $\overline{RASIN}$ during refresh	Figure 3	50			50			ns
t_{RST}	Counter reset pulse width	Figure 3	70			70			ns
$t_{RFCKL,H}$	Minimum pulse width of RFCK	Figure 6	100			100			ns
T	Period of $\overline{RAS}$ generator clock	Figure 6	100			100			ns
t_{RGCKL}	Minimum pulse width low of RGCK	Figure 6	35			35			ns
t_{RGCKH}	Minimum pulse width high of RGCK	Figure 6	35			35			ns
t_{CSRL}	$\overline{CS}$ low to access $\overline{RASIN}$ low	See Mode 5 description	10			10			ns
t_{RFSRG}	$\overline{RFSH}$ low set-up to RGCK low (Mode 1)	See Mode 1 description	35			35			ns
t_{RQHRF}	$\overline{RFSH}$ hold time from $\overline{RFRQ}$ (RF I/O)	Figure 6	2T			2T			ns

Electrical Characteristics: $V_{CC} = 5.0V \pm 5.0\%$, $0°C \leq T_A \leq 75°C$ Typicals are for $V_{CC} = 5V$, $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C	Input clamp voltage	V_{CC} = MIN, $I_C = -12mA$		−0.8	−1.2	V
I_{IH1}	Input high current for ADS, R/C only	$V_{IN} = 2.5V$		2.0	100	μA
I_{IH2}	Input high current for other inputs, except RF I/O	$V_{IN} = 2.5V$		1.0	50	μA
I_{IRSI}	Output load current for RF I/O	$V_{IN} = 0.5V$, output high		−1.5	−2.5	mAV
I_{ICTL}	Output load current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	$V_{IN} = 0.5V$, chip deselct		−1.5	−2.5	mA
I_{IL1}	Input low current for ADS, R/$\overline{C}$ only	$V_{IN} = 0.5V$		−0.1	−1.0	mA
I_{IL2}	Input low current for other inputs, except RF I/O	$V_{IN} = 0.5V$		−0.05	−0.5	mA
V_{IL}**	Input low threshold				0.8	V
V_{IH}**	Input high threshold		2.0			V
V_{OL1}	Output low voltage, except RF I/O	$I_{OL} = 20mA$		0.3	0.5	V
V_{OL2}	Output low voltage for RF I/O	$I_{OL} = 10mA$		0.3	0.5	V
V_{OH1}	Output high voltage, except RF I/O	$I_{OH} = -1mA$	2.4	3.5		V
V_{OH2}	Output high voltage for RF I/O	$I_{OH} = -100\mu A$	2.4	3.5		V
I_{1D}	Output high drive current, except RF I/O	$V_{OUT} = 0.8V$ (Note 3)		−200		mA
I_{0D}	Output low drive current, except RF I/O	$V_{OUT} = 2.7V$ (Note 3)		200		mA
I_{OZ}	Three-state output current (address outputs)	$0.4V \leq V_{OUT} \leq 2.7V$, CS = 2.0V, Mode 4	−50	1.0	50	μA
I_{CC}	Supply current	V_{CC} = MAX		250	325	mA
C_{IN}	Input capacitance ADS, R/$\overline{C}$	$T_A = 25°C$		8		pF
C_{IN}	Input capacitance all other inputs	$T_A = 25°C$		5		pF

** These are absolute voltages with respect to pins 13 or 38 on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

Switching Characteristics: V_{CC} = 5.0V ± 5.0%, 0°C ≤ T_A ≤ 75°C See Figure 12 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for V_{CC} = 5V, T_A = 25°C.

SYMBOL	ACCESS PARAMETER	FIGURE	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
t_{RHA}	Row address held from column select	Figure 4	10			10			ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10	95	125	160	75	100	130	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10, 11	80	105	140	65	90	115	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10	50	63	80	50	63	80	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10, 11	40	48	60	40	48	60	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10		98	125		75	100	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10, 11		78	105		65	85	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 5)	Figures 7, 10		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ output delay (Mode 6)	Figures 7, 10		40	65		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ output delay Mode 6)	Figure 11	40	54	70	40	54	70	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 5)	Figures 7, 10		90	120		80	105	ns
t_{RCV}	$\overline{RASIN}$ to column address valid (Mode 6)	Figures 7, 10, 11		75	105		70	90	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4, 5, 7, 10, 11	20	27	35	20	27	35	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay	Figures 4, 5, 7, 10, 11	15	23	32	15	23	32	ns
t_{APDL}	Address input to output low delay	Figures 4, 5, 7, 10, 11		25	40		25	40	ns
t_{APDH}	Address input to output high delay	Figures 4, 5, 7, 10, 11		25	40		25	40	ns
t_{SPDL}	Address strobe to address output low	Figures 4, 5		40	60		40	60	ns
t_{SPDH}	Address strobe to address output high	Figures 4, 5		40	60		40	60	ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 5	15	25	30	15	25	30	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ output delay	Figure 5	15	30	60	15	30	60	ns
t_{CRS}	$\overline{CASIN}$ setup time to $\overline{RASIN}$ high (Mode 6)	Figure 11	35			35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ delay (R/C low in Mode 4)	Figure 5	32	41	58	32	41	58	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ delay	Figure 5	25	39	50	25	39	50	ns
t_{RCC}	Column select to column address valid	Figure 4		40	58		40	58	ns
t_{RCR}	Row select to row address valid	Figures 4, 5		40	58		40	58	ns
t_{RAH}	Row address hold time (Mode 5)	Figures 7, 10	30			20			ns
t_{RAH}	Row address hold time (Mode 6)	Figures 7, 10, 11	20			12			ns
t_{ASC}	Column address setup time (Mode 5)	Figures 7, 10	8			3			ns
t_{ASC}	Column address setup time (Mode 6)	Figures 7, 10, 11	6			3			ns
t_{DIF1}	Maximum ($t_{RPDL} - t_{RHA}$) (Mode 4)				15			15	ns
t_{DIF2}	Maximum ($t_{RCC} - t_{CPDL}$) (Mode 4)				15			15	ns

SYMBOL	REFRESH PARAMETER	TEST CONDITIONS	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
t_{FRQL}	RFCK low to forced $\overline{RFRQ}$ low	C_L = 50 pF, Figure 6		20	30		20	30	ns
t_{FRQH}	RGCK low to force $\overline{RFRQ}$ high	C_L = 50pF, Figure 6		50	75		50	75	ns
t_{RGRL}	RGCK low to $\overline{RAS}$ low	Figure 6	50	65	95	50	65	95	ns
t_{RGRH}	RGCK low to $\overline{RAS}$ high	Figure 6	40	60	85	40	60	85	ns
t_{RFRH}	$\overline{RFSH}$ high to $\overline{RAS}$ high (encoding forced RFSH)	See Mode 1 description	55	80	110	55	80	110	ns
t_{CSCT}	$\overline{CS}$ high to $\overline{RFSH}$ counter valid	Figure 6		55	70		55	70	ns
t_{CTL}	RF I/O low to counter outputs all low	Figure 3			100			100	ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figures 3, 6	35	50	70	35	50	70	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ delay during refresh	Figures 3, 6	30	40	55	30	40	55	ns
t_{RFLCT}	$\overline{RFSH}$ low to counter address valid	$\overline{CS}$ = X, Figures 3, 6, 8		47	60		47	60	ns
t_{RFHRV}	$\overline{RFSH}$ high to row address valid	Figures 3, 6		45	60		45	60	ns
t_{ROHNC}	$\overline{RAS}$ high to new count valid	Figures 3, 8		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ low to end-of-count low	C_L = 50pF, Figure 3			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ high to end-of-count high	C_L = 50pF, Figure 3			80			80	ns
t_{RGEOB}	RGCK low to end-of-burst low	C_L = 50pF, Figure 8			95			95	ns
t_{MCEOB}	Mode change to end-of-burst high	C_L = 50pF, Figure 8			75			75	ns

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Switching Characteristics: (Cont'd)

SYMBOL	ACCESS PARAMETER	TEST CONDITIONS	'S409 MIN	'S409 TYP	'S409 MAX	'S409-2 MIN	'S409-2 TYP	'S409-2 MAX	UNIT
	THREE-STATE PARAMETER								
t_{ZH}	$\overline{CS}$ low to address output high from Hi	Figures 6, 12 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ high to address output Hi-Z from high	C_L = 15pF, Figures 6,12 R2 = 1k, S1 Open		20	40		20	40	ns
t_{ZL}	$\overline{CS}$ low to address output low from Hi-Z	Figures 6, 12 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ high to address output Hi-Z from low	C_L = 15pF, Figures 6,13 R1 = 1k, S2 Open		25	50		25	50	ns
t_{HZH}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0}$-3) high from Hi-Z high	Figures 6,12 R2 = 750Ω, S1 open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0}$-3) Hi-Z high from high	C_L = 15pF R2 = 750Ω, S1 open		40	75		40	75	ns
t_{HZL}	$\overline{CS}$ low to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0}$-3) low from Hi-Z high	Figure 12 S1, S2 Open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ high to control output ($\overline{WE}$, $\overline{CAS}$, ($\overline{RAS0}$-3) Hi-Z high from low	C_L = 15pF, Figure 12 R2 = 750Ω, S1 open		50	80		50	80	ns

*Internally the device contains a 3K resistor in series with a Schottky Diode to V_{CC}.

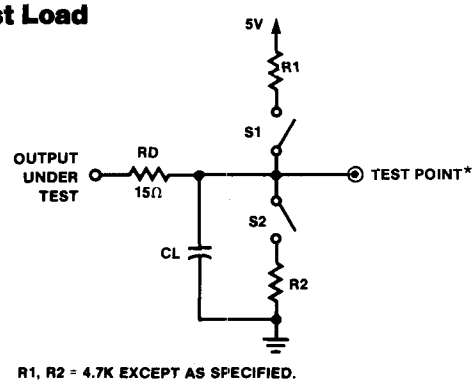
Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8. C_L = 500pF; RAS0-RAS3, C_L = 150pF; CAS C_L = 600pF unless otherwise noted.

Note 2: All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F$ = 2.5 ns, f = 2.5 MHz. t_{PW} = 200 ns. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Test Load



R1, R2 = 4.7K EXCEPT AS SPECIFIED.

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

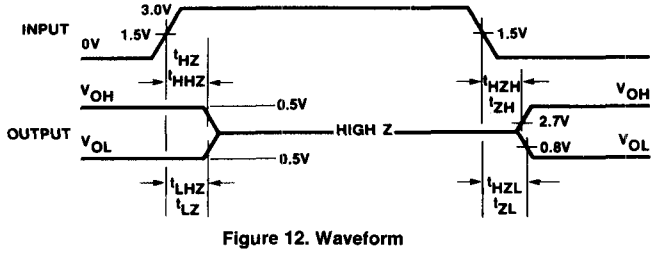


Figure 12. Waveform

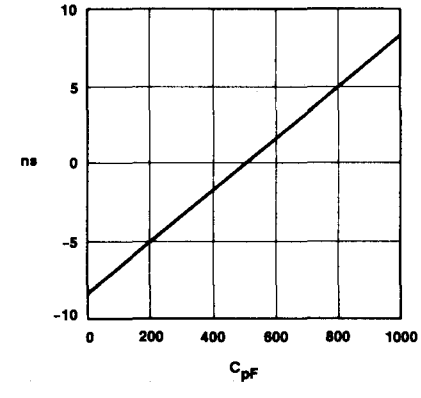


Figure 13. Change in Propagation Delay vs Loading

Capacitance Relative to a 500 pF Load

Applications

The 74S409 Dynamic RAM Controller provides all the address and control signals necessary to access and refresh dynamic RAMs. Since the 74S409 is not compatible with a specific bus or microprocessor, an interface is often necessary between the 74S409 and the system. A general application using PAL to implement the interface and two additional chips to provide refresh clock and chip select is shown in Figure 14.

The 74S409 operating modes may vary from application to application. For efficient refresh it is recommended to use mode 1 and mode 5 to take advantage of the hidden (transparent) refresh with forced refresh backup.

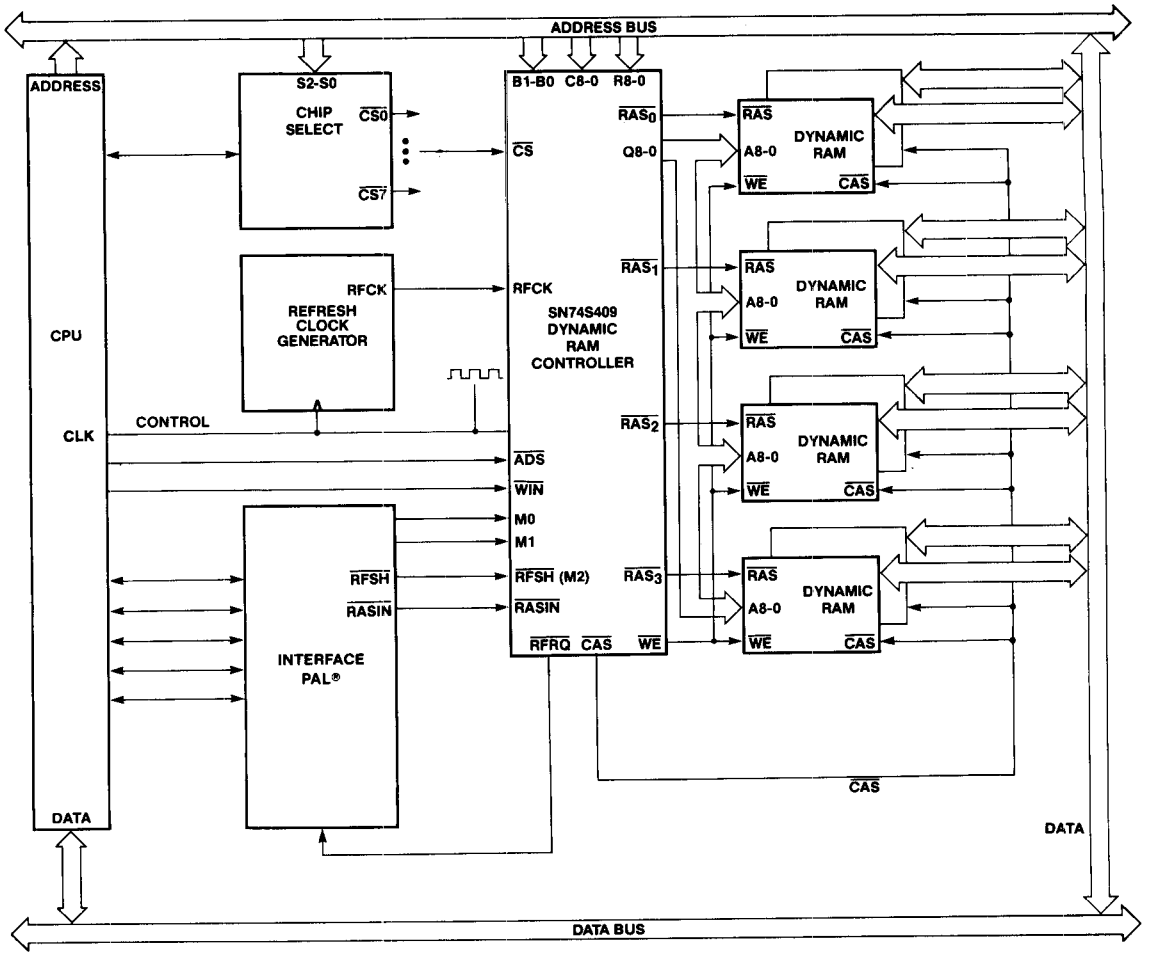


Figure 14. 74S409 in General Application