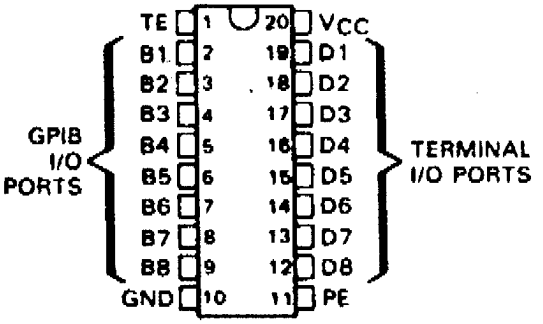
OCTAL GENERAL-PURPOSE
INTERFACE BUS TRANSCEIVER

D2525

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Power-Up/Power-Down Protection (Glitch-Free)
- High-Speed, Low-Power Schottky Circuitry
- Low-Power Dissipation . . . 72 mW Max per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device is Powered Down (V_{CC} = 0)

DW, J, OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLES

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z†
X	L	X	Z†

EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = High-impedance state.

† This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

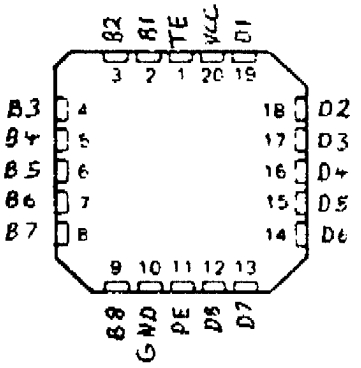
description

The SN75160B 8-channel general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of passive-pullup outputs when Pullup Enable (PE) is low, and of three-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current.

Output glitches during power-up and power-down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0 volts. When combined with the SN75161B or SN75162B management bus transceivers, the pair provides the complete 16-wire interface for the IEEE 488 bus.

The SN75160B is characterized for operation from 0°C to 70°C.
−55°C to 100°C.

SN75160B
SN55160B . . . FK Package
(TOP VIEW)



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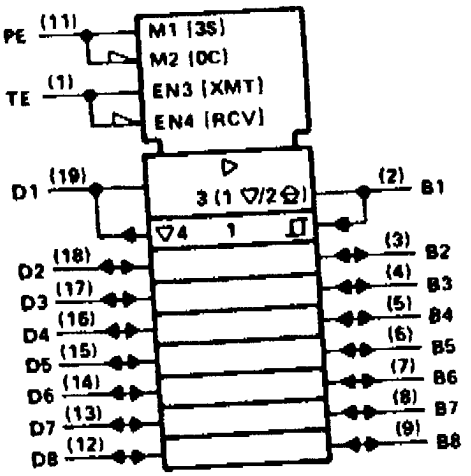
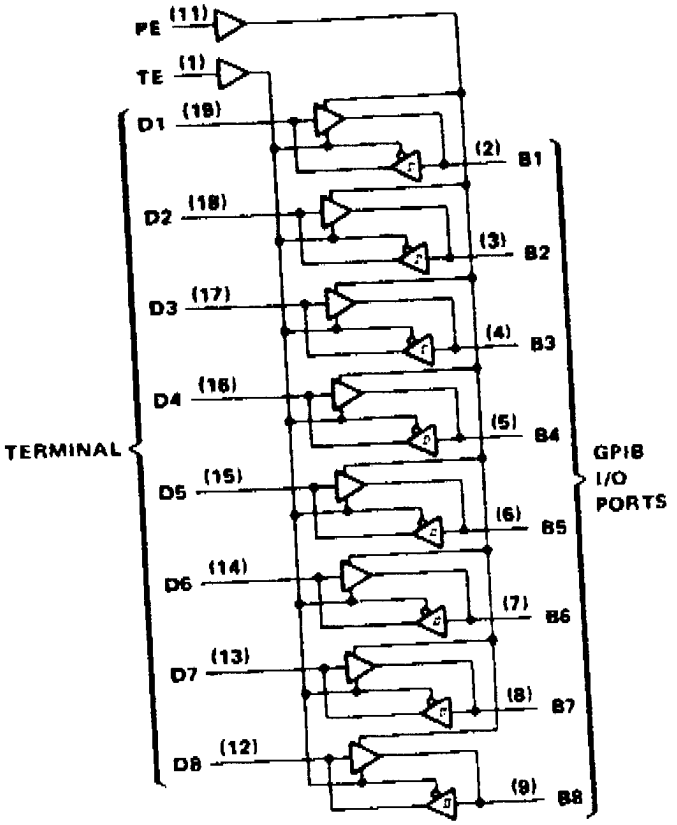
logic symbol†



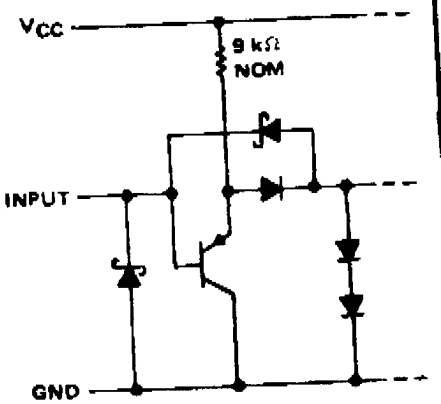
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
⏚ Designates passive-pullup outputs.

logic diagram (positive logic)

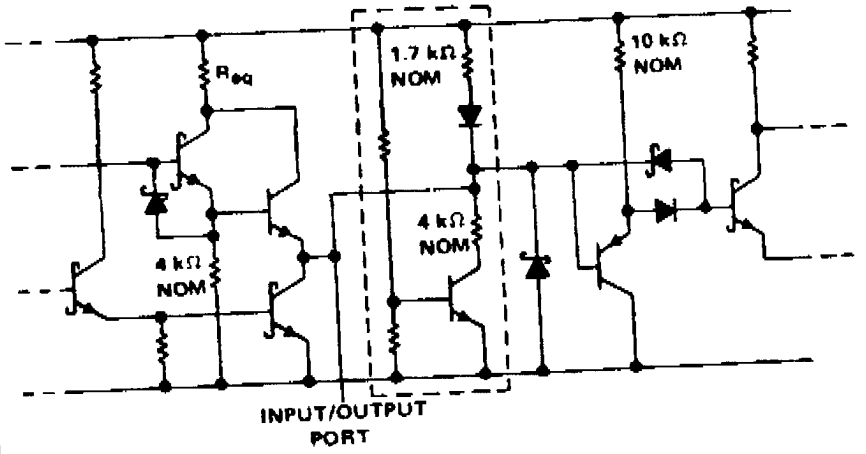


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
~~DW package~~ . . . . . ~~1125 mW~~
J package . . . . . 1375 mW
FK ~~N~~ package . . . . . 1375 ~~1150~~ mW
Operating free-air temperature range . . . . . -55°C ~~0°C~~ to ~~70°C~~ 100°C
Storage temperature range . . . . . -65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 60 seconds: J package . . . . . 300°C
~~Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . . 260°C~~

NOTES 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate ~~the DW package at the rate of 9.0 mW/°C~~ the FK ~~N~~ package at the rate of ~~9.2~~ 11.0 mW/°C, and the J package at the rate of 11.0 mW/°C. In the J package and FK, SN75160B chips are alloy mounted

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}, PE + TE		2			V
Low-level input voltage, V_{IL}, PE & TE				0.8	V
High-level output current, I_{OH}	Bus ports with pull-ups active			-5.2	mA
	Terminal ports			-800	µA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		~~0~~ -55		~~70~~ 100	°C

HIGH-level input voltage, VIH, Bus & Terminal	25°C	2	V
	Full Range	2.1	V
Low-level input voltage, VIL, Bus & Terminal	25°C	.8	V
	Full Range	.7	V

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA, V_{CC} = Min			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus	V_{CC} = 5 V		0.4	0.65		V
V_{OH}	High-level output voltage	Terminal	I_{OH} = −800 µA,	TE at 0.8 V, V_{CC} = Min	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V, V_{CC} = Min	2.4	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V, V_{CC} = Min		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V, V_{CC} = Min		0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V, V_{CC} = Max			0.2	100	µA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V, V_{CC} = Max			0.1	20	µA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V, V_{CC} = Max			−10	−100	µA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled, V_{CC} = 5 V	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled, V_{CC} = 5 V	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			+40	µA
I_{OS}	Short-circuit output current	Terminal	V_{CC} = Max		−15	−35	−75	mA
		Bus	V_{CC} = Max		−25	−50	−125	
I_{CC}	Supply current		No load, V_{CC} = Max,	Receivers low and enabled		70	90	mA
				Drivers low and enabled		85	110	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V to 0 V, f = 1 MHz	$V_{I/O}$ = 0 to 2 V,		30		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		10	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					15	22	
t_{PZH}	Output enable time to high level	TE	Bus	See Figure 3		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level					22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	See Figure 4		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pull-up enable time	PE	Bus	See Figure 5		15	22	ns
t_{dis}	Output pull-up disable time					13	20	

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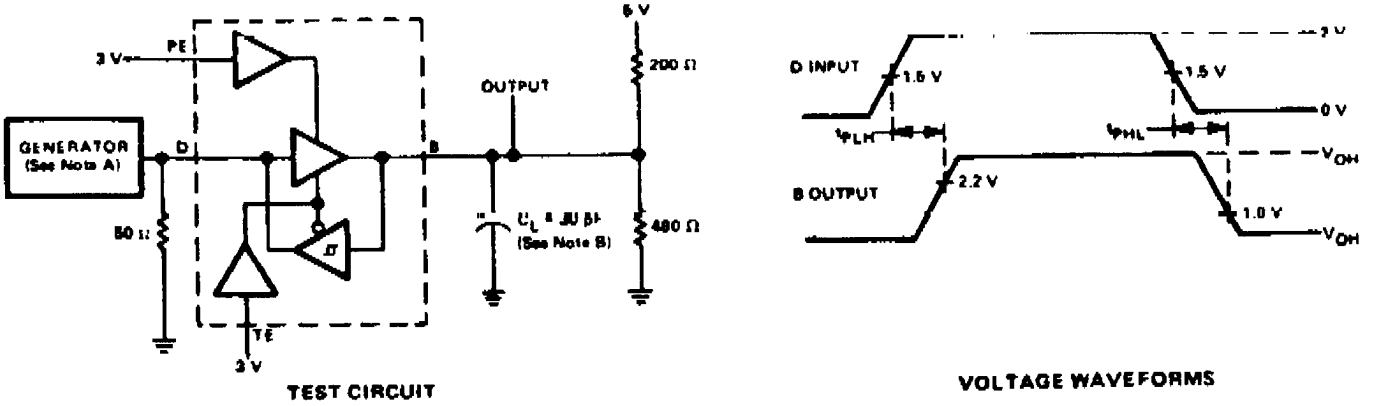
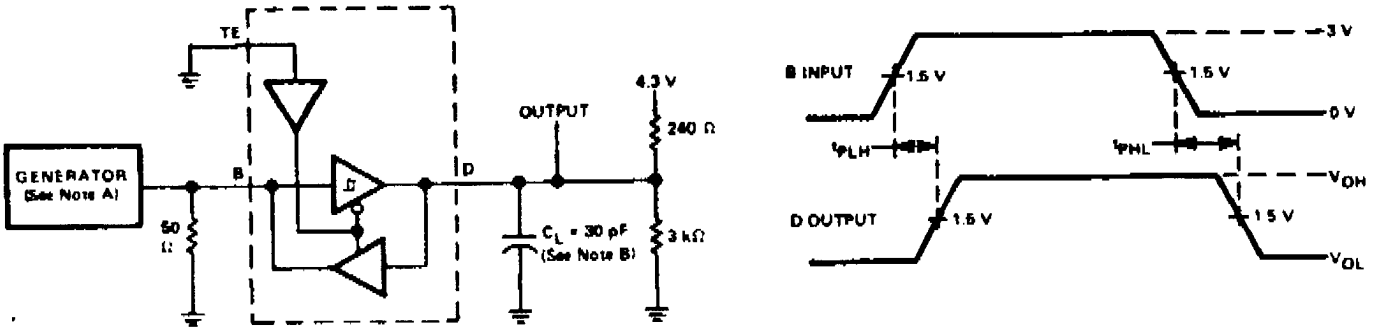
PARAMETER MEASUREMENT INFORMATION



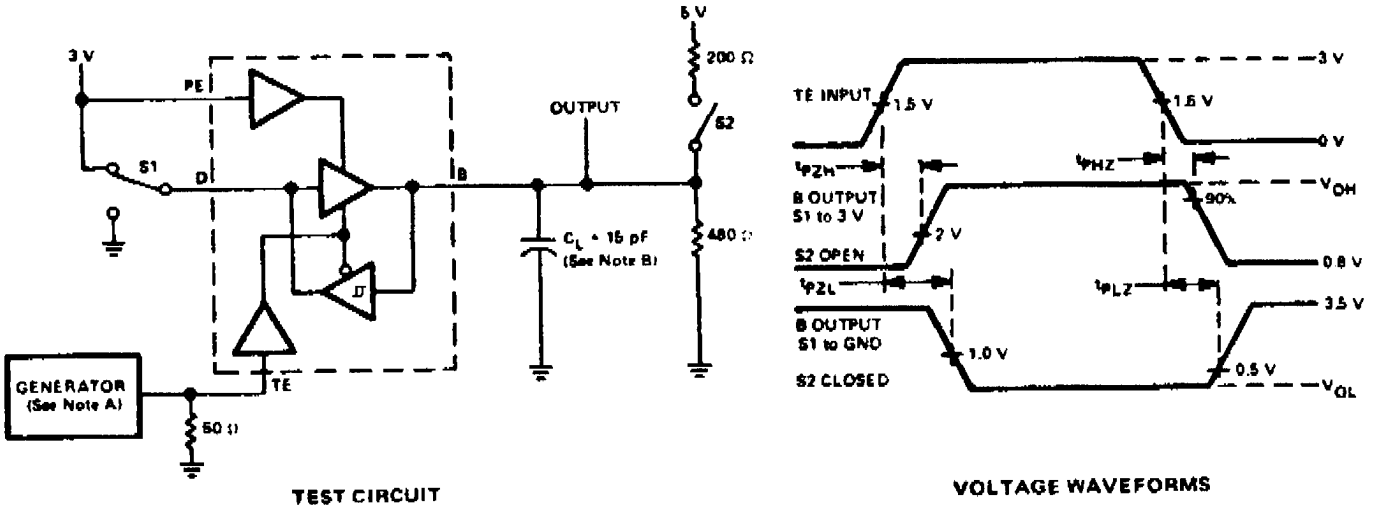
TEST CIRCUIT — VOLTAGE WAVEFORMS

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES



TEST CIRCUIT — VOLTAGE WAVEFORMS

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES



TEST CIRCUIT — VOLTAGE WAVEFORMS

FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.

B. C_L includes probe and jig capacitance.

6 ns

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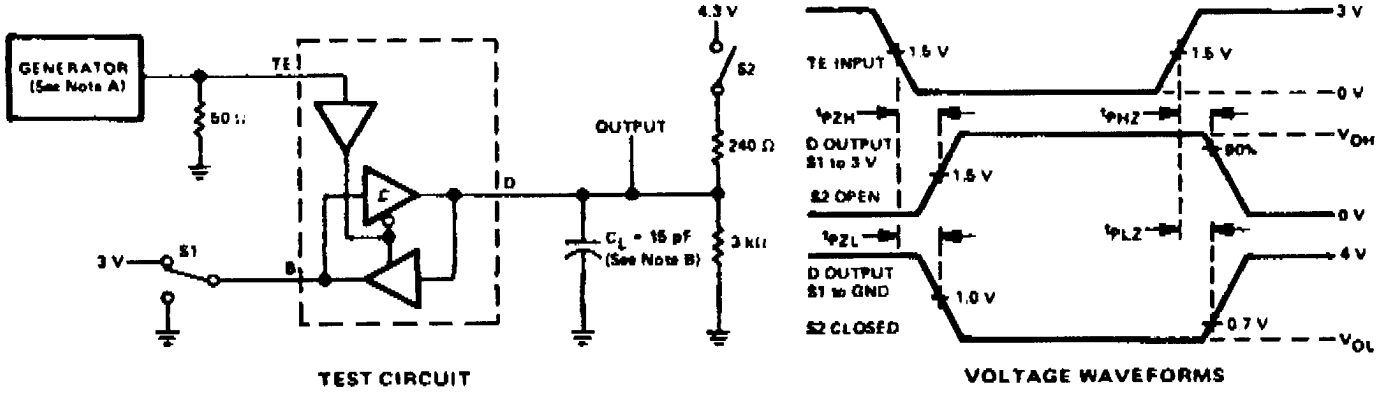
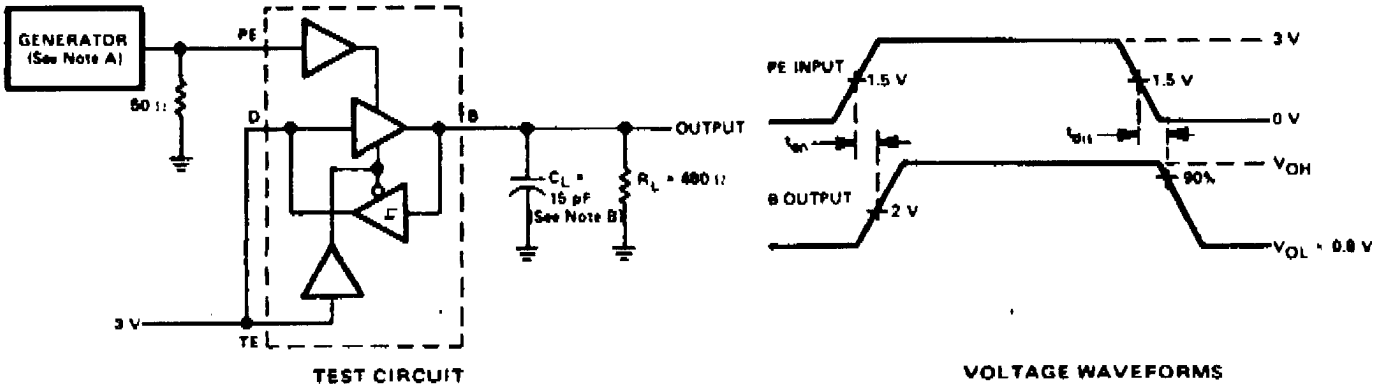
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance

6 ns

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TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

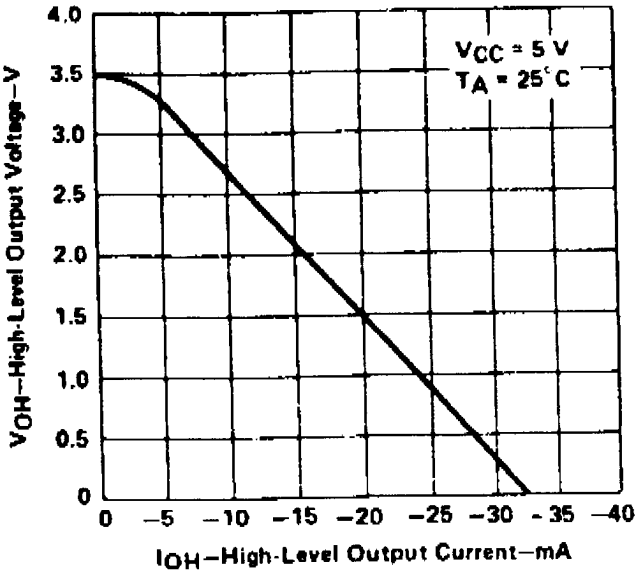

FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

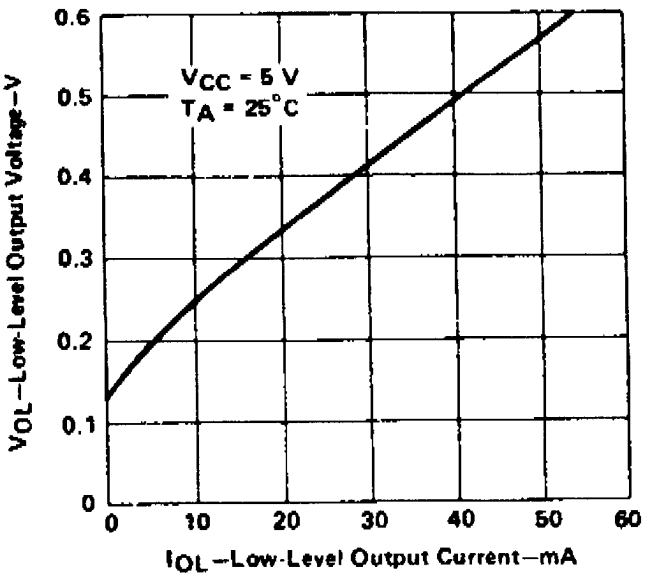

FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

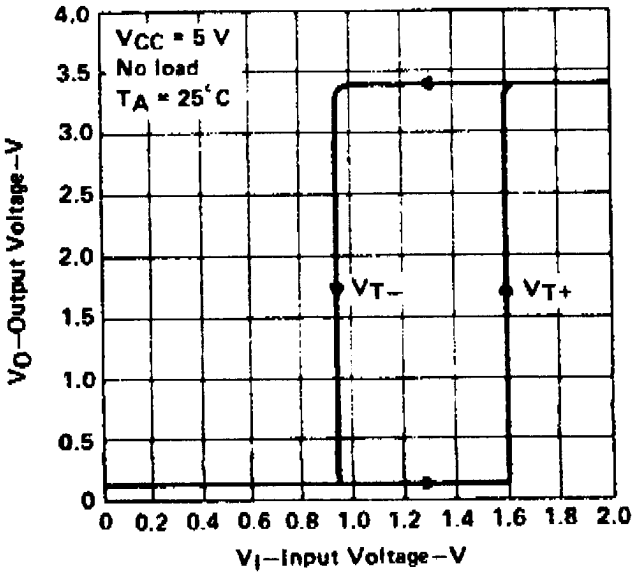

FIGURE 8

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TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

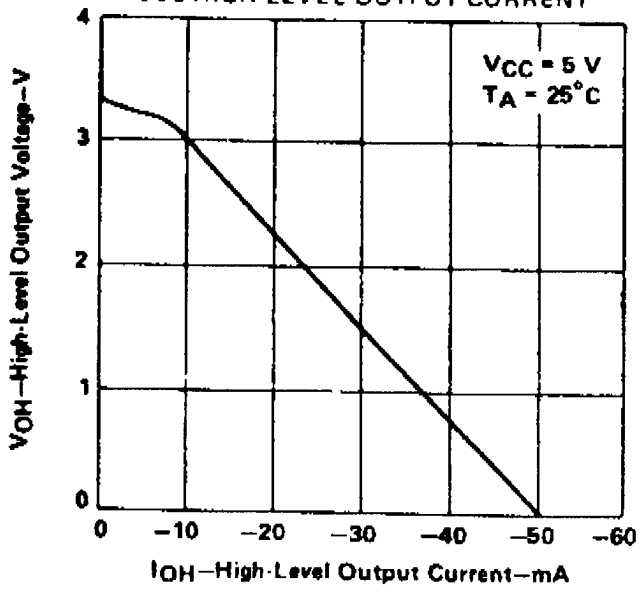

FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

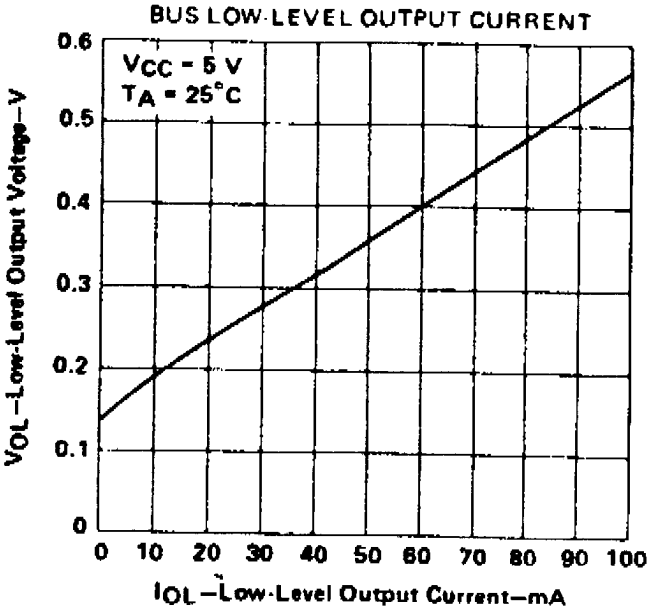

FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

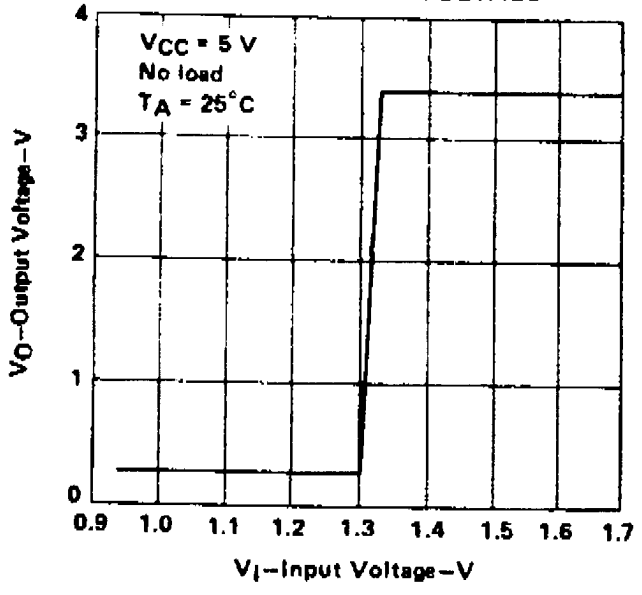

FIGURE 11

BUS CURRENT
vs
BUS VOLTAGE

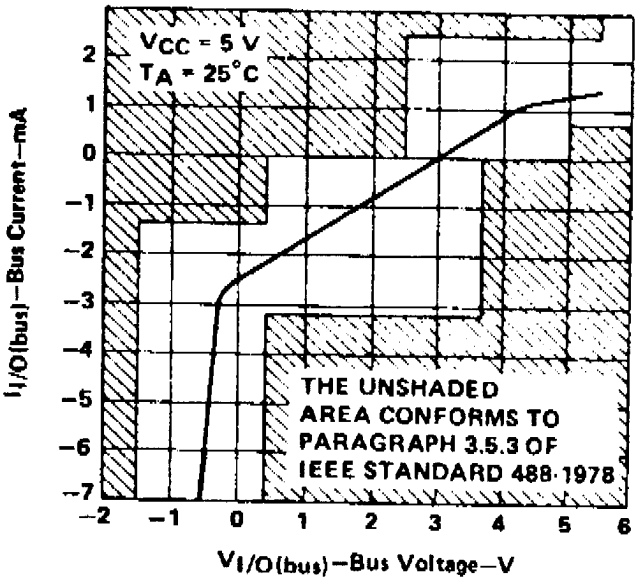

FIGURE 12

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