

TOSHIBA MOS MEMORY PRODUCTS

32,768 WORD×8 BIT STATIC RAM
SILICON GATE CMOS

TC55257APL-85/APL-10/APL-12
TC55257AFL-85/AFL-10/AFL-12

PRELIMINARY

DESCRIPTION

The TC55257APL/AFL is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a operating current of 5mA/MHz (Typ.) and minimum cycle time of 85ns. When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 2 μ A typically. The TC55257 APL/AFL has two control inputs. Chip enable

($\overline{CE}$) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The TC55257APL/AFL is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

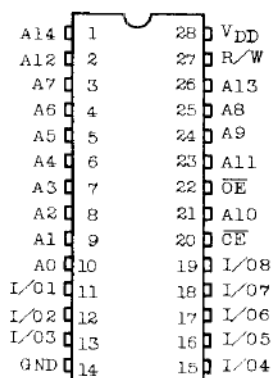
FEATURES

- Low Power Dissipation
27.5mW/MHz (Typ.) Operating
- Standby Current
100 μ A (Max.): TC55257APL-85/AFL-85
APL-10/AFL-10
APL-12/AFL-12
- 5V Single Power Supply
- Power Down Feature: $\overline{CE}$

- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Access Time

	TC55257APL-85 TC55257AFL-85	TC55257APL-10 TC55257AFL-10	TC55257APL-12 TC55257AFL-12
Access Time (Max.)	85ns	100ns	120ns
Chip Enable Access Time (Max.)	85ns	100ns	120ns
Output Enable Time (Max.)	45ns	50ns	60ns

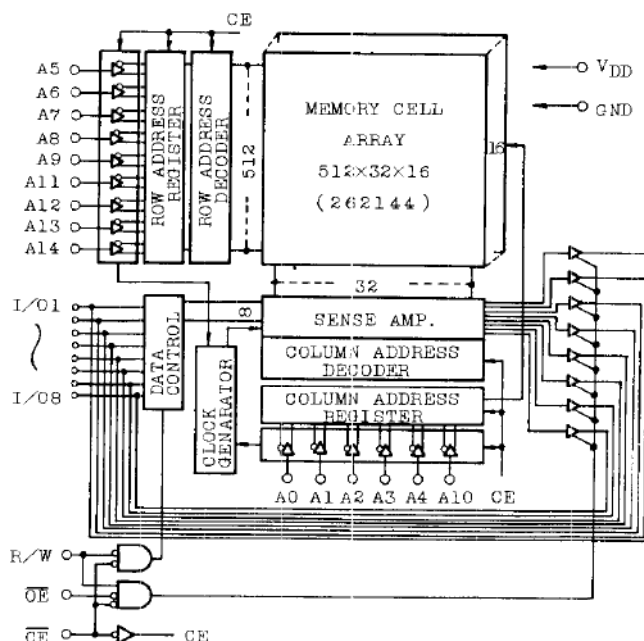
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O8	Data Inputs/Outputs
V _{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



TC55257APL-85/APL-10/APL-12

TC55257AFL-85/AFL-10/AFL-12

OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	L	H	D _{OUT}	I _{DD0}
Write	L	*	L	D _{IN}	I _{DD0}
Output Deselect	L	H	H	High-Z	I _{DD0}
Standby	H	*	*	High-Z	I _{DDs}

*) H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{I/O}	Input and Output Voltage	-0.5 ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0	W
T _{solder}	Soldering Temperature	260 ± 10	°C • sec
T _{strg}	Storage Temperature	-55 ~ 150	°C
T _{opr}	Operating Temperature	0 ~ 70	°C

*) -3.0V at pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	—	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	-0.3*	—	0.8	V
V _{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

*) -3.0V at pulse width 50ns

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D.C. and OPERATING CHARACTERISTICS (Ta = 0 ~ 70°C, VDD = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
IIL	Input Leakage Current	VIN = 0 ~ VDD	—	—	± 1.0	μA
IOH	Output High Current	VOH = 2.4V	—10	—	—	mA
IOL	Output Low Current	VOL = 0.4V	4.0	—	—	mA
ILO	Output Leakage Current	CE = VIH or R/W = VIL or OE = VIH VOUT = 0 ~ VDD	—	—	± 1.0	μA
IDD01	Operating Current	VDD = 5.5V CE = VIL, R/W = VIH Other Input = VIH/VIL IOUT = 0mA	tcycle = 1μs	—	10	—
			tcycle = Min. cycle	—	—	70
IDD02	Operating Current	VDD = 5.5V CE = 0.2V, R/W = VDD-0.2V Other Input = VDD-0.2V/0.2V IOUT = 0mA	tcycle = 1μs	—	5	—
			tcycle = Min. cycle	—	—	60
IDDs1	Standby Current	CE = VIH	—	—	3	mA
IDDs2	Standby Current	CE = VDD-0.2V VDD = 2.0 ~ 5.5V	Ta = 0 ~ 70°C	—	2	100
						μA

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
CIN	Input Capacitance	VIN = GND	10	pF
COUT	Output Capacitance	VOUT = GND	10	pF

Note: This parameter periodically sampled is not 100% tested.

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A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC55257APL-85 TC55257AFL-85		TC55257APL-10 TC55257AFL-10		TC55257APL-12 TC55257AFL-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	85	—	100	—	120	—	ns
t _{ACC}	Address Access Time	—	85	—	100	—	120	
t _{CO}	CE Access Time	—	85	—	100	—	120	
t _{OE}	Output Enable to Output in Valid	—	45	—	50	—	60	
t _{COE}	Chip Enable (CE) to Output in Low-Z	10	—	10	—	10	—	
t _{OEE}	Output Enable to Output in Low-Z	5	—	5	—	5	—	
t _{OD}	Chip Enable (CE) to Output in High-Z	—	30	—	50	—	60	
t _{ODO}	Output Enable to Output in High-Z	—	30	—	40	—	50	
t _{OH}	Output Data Hold Time	5	—	10	—	10	—	

Write Cycle

SYMBOL	PARAMETER	TC55257APL-85 TC55257AFL-85		TC55257APL-10 TC55257AFL-10		TC55257APL-12 TC55257AFL-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	85	—	100	—	120	—	ns
t _{WP}	Write Pulse Width	60	—	70	—	80	—	
t _{CW}	Chip Selection to End of Write	65	—	90	—	100	—	
t _{AS}	Address Set up Time	0	—	0	—	0	—	
t _{WR}	Write Recovery Time	5	—	5	—	5	—	
t _{ODW}	R/W to Output High-Z	—	30	—	50	—	60	
t _{OEW}	R/W to Output Low-Z	10	—	10	—	10	—	
t _{DS}	Data Set up Time	40	—	40	—	50	—	
t _{DH}	Data Hold Time	0	—	0	—	0	—	

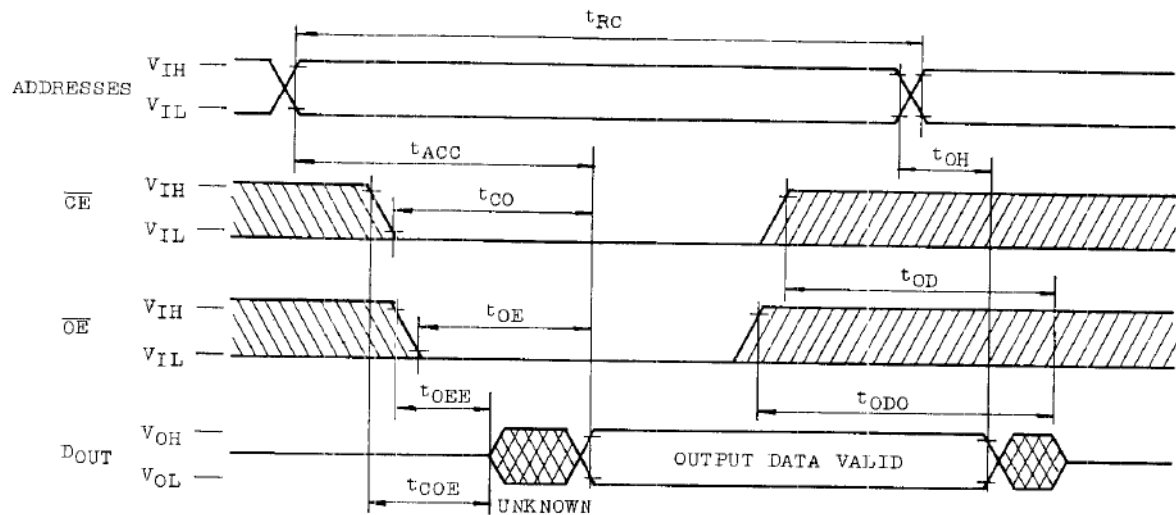
A.C. TEST CONDITIONS

Output Load : 100pF + 1TTL Gate
 Input Pulse Level : 0.6V, 2.4V
 Timing Measurement : 0.8V, 2.2V
 Reference Level : 0.8V, 2.2V
 t_r, t_f : 5ns

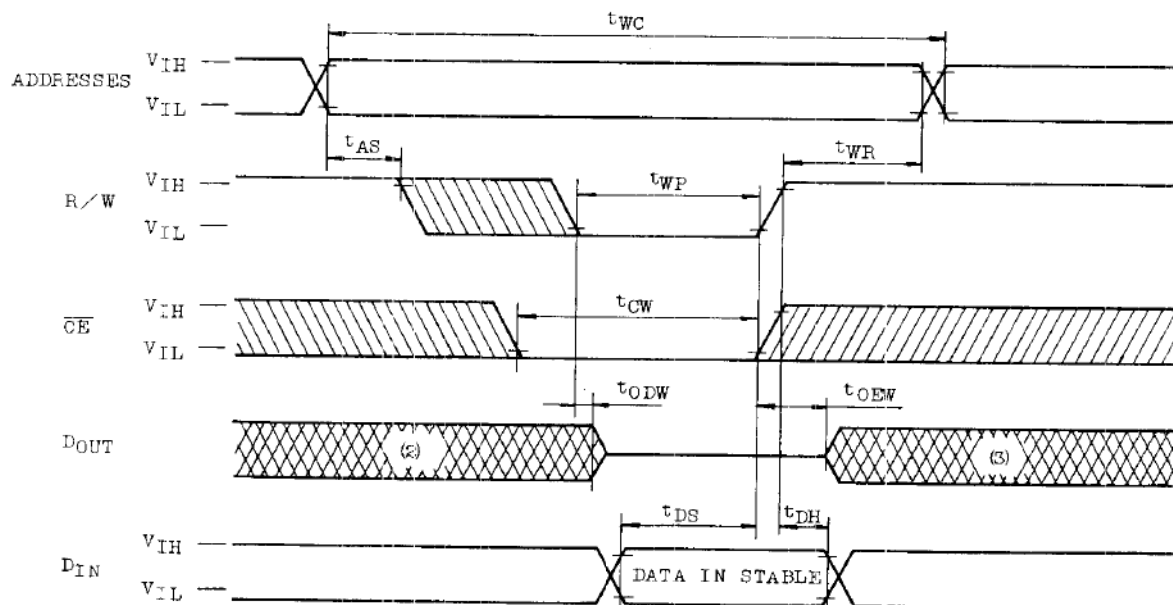
TC55257APL-85/APL-10/APL-12 TC55257AFL-85/AFL-10/AFL-12

TIMING WAVEFORMS

• READ CYCLE⁽¹⁾

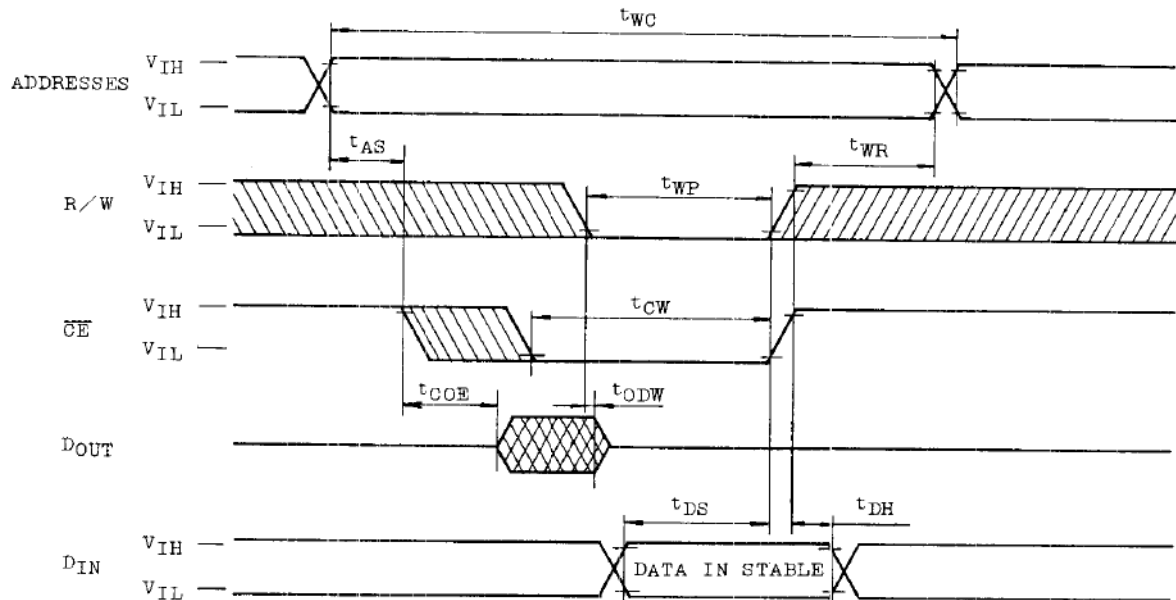


• WRITE CYCLE 1⁽⁴⁾ (R/W Controlled Write)



TC55257APL-85/APL-10/APL-12 TC55257AFL-85/AFL-10/AFL-12

• WRITE CYCLE 2⁽⁴⁾ ($\overline{CE}$ Controlled Write)



NOTE: 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}$ low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, Output remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

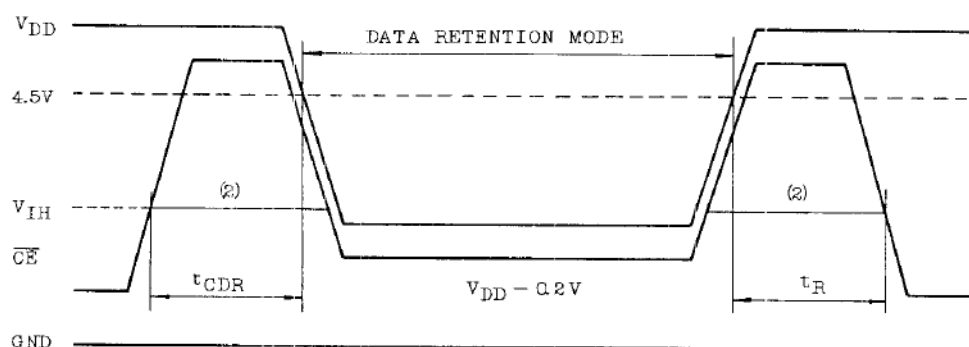
TC55257APL-85/APL-10/APL-12 TC55257AFL-85/AFL-10/AFL-12

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I _{DDS2}	Standby Supply Current	V _{DH} = 3.0V	—	50	μA
		V _{DH} = 5.5V	—	100	
t _{CDR}	Chip Deselection to Data Retention Mode	0	—	—	μs
t _R	Recovery Time	t _{RC} (1)	—	—	

Note (1): Read Cycle Time.

• $\overline{\text{CE}}$ Controlled Data Retention Mode

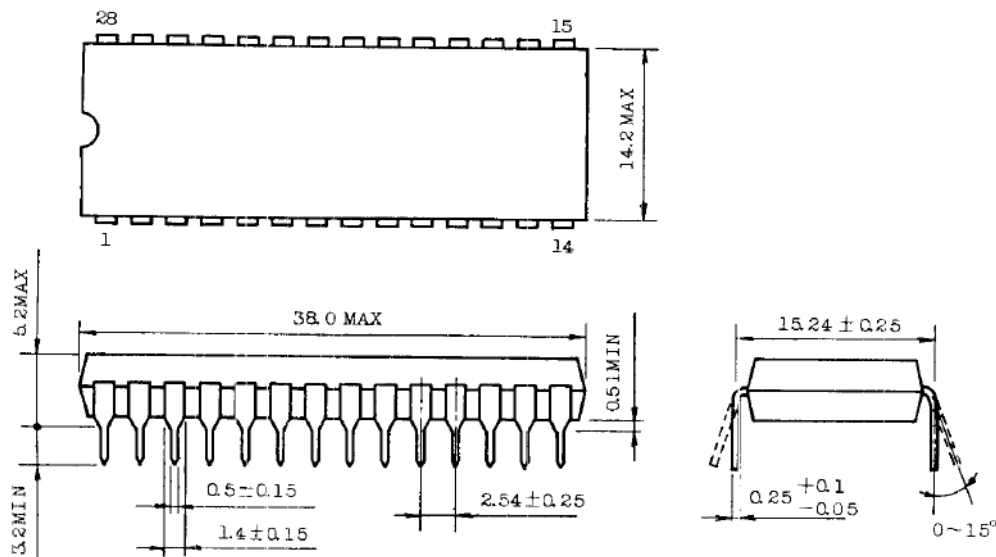


NOTE (2): If the V_{IH} of $\overline{\text{CE}}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

TC55257APL-85/APL-10/APL-12 **TC55257AFL-85/AFL-10/AFL-12**

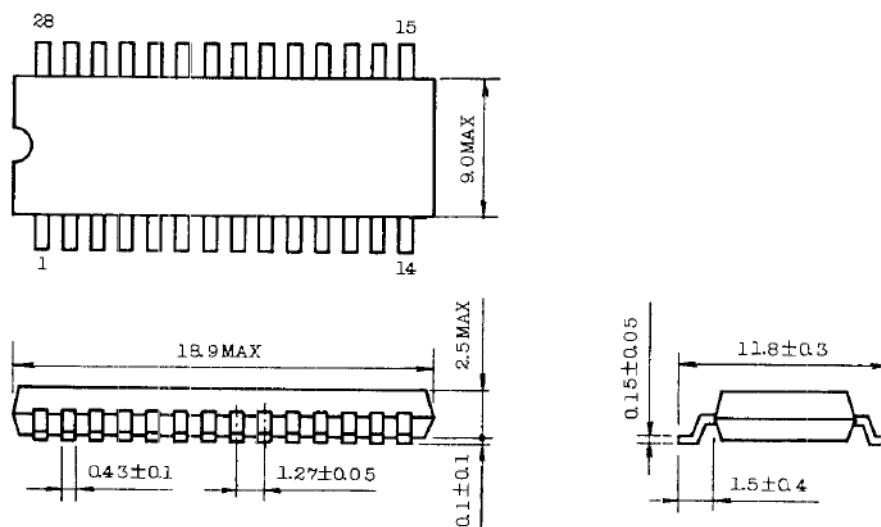
● DIP 28 PIN OUTLINE DRAWING (6D28A-P)

Unit in mm



NOTE: Lead pitch is 2.54 and tolerance is ± 0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

● MFP 28 PIN OUTLINE DRAWING (F28GA-P)



NOTE: Lead pitch is 1.27 and tolerance is ± 0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.