

# DATA SHEET

## **TDA4691** Sync Processor with Clock (SPC)

Preliminary specification  
File under Integrated Circuits, IC02

September 1993

## Sync Processor with Clock (SPC)

TDA4691

## FEATURES

- Sync processor for horizontal (H) and vertical (V) sync pulses generated by internal 13.5 MHz oscillator
- Stable 'On Screen Display (OSD)', if no input signal is present with free running internal oscillator; automatic turn over to locked oscillator, if input signal is available
- External clock oscillator can be used
- Standard 50/60 Hz signals are identified automatically
- Additional outputs for 13.5 MHz, composite sync, 50//60 Hz identification, signal identification (mute), super-sandcastle 12 V
- TTL compatible outputs (H, V, composite sync and 13.5 MHz)
- 3 different time constants for the PHI1 PLL: fast, normal and slow ( $T_1$ ,  $T_2$  and  $T_3$ ). Fast and normal time constant are set independent from each other
- Start of H-pulse definable by application
- Digital interference reduction for H and V signals
- Digital noise detector
- Time correction of non-standard H-pulses and equalizing pulses for optimum PLL control.

## GENERAL DESCRIPTION

The TDA4691 is a bipolar integrated circuit for sync processing in 50/100 and 60/120 Hz TV sets, preferably in conjunction with the programmable deflection controller TDA9150. A line locked 13.5 MHz clock with several dividers and logic circuitry is available generating the horizontal and vertical sync outputs. The device can be assembled in a DIL20 or SO20 package.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_{P2}$	supply voltage		4.5	5.0	5.5	V
$I_{P2}$	supply current		–	–	30	mA
$V_{P1}$	supply voltage		7.2	8.0	8.8	V
$I_{P1}$	supply current		–	–	30	mA
$P_{tot}$	total power dissipation		–	260	430	mW
<b>Inputs</b>						
$V_{20}$	input voltage	$R_G = 1\text{ k}\Omega$	–	1	2	V
<b>Outputs</b>						
$V_4$	signal identification voltage	no signal; 1 mA	–	–	0.3	V
		signal	open collector	–	$V_{P1}$	V
$V_7$	50/60 Hz voltage	50 Hz; 1 mA	–	–	0.3	V
		60 Hz	open collector	–	$V_{P1}$	V
$V_{10}$	vertical output voltage	HIGH; –1 to 0 mA	2.7	–	$V_{P2}$	V
		LOW; 2 mA	–	–	0.8	V
$V_{11}$	horizontal output voltage	HIGH; –1 to 0 mA	2.7	–	$V_{P2}$	V
		LOW; 2 mA	–	–	0.8	V
$V_{13}$	clock output voltage	HIGH; –1 to 0 mA	2.7	–	$V_{P2}$	V
		LOW; 2 mA	–	–	0.8	V

## ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4691	20	DIL	plastic	SOT146 <sup>(1)</sup>
TDA4691T	20	SO	plastic	SOT163 <sup>(2)</sup>

## Note

1. SOT146-1; 1996 December 9.
2. SOT4163-1; 1996 December 9.

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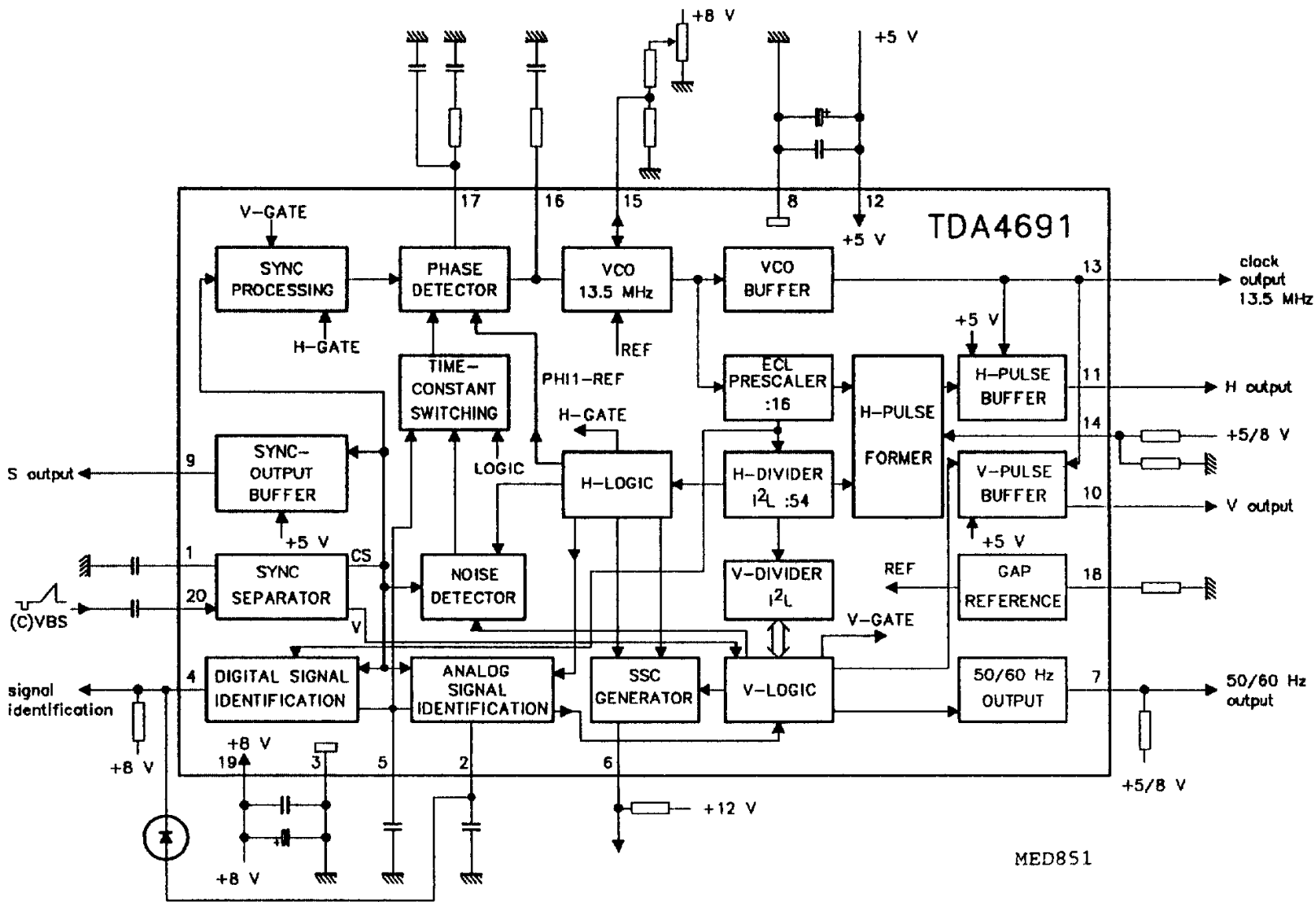


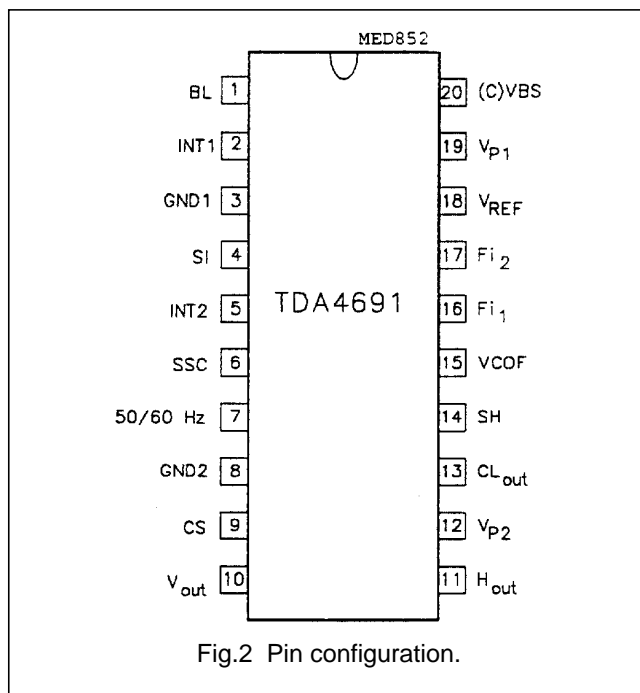
Fig.1 Block diagram.

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## PINNING

SYMBOL	PIN	DESCRIPTION
BL	1	black level storage of sync separator
INT1	2	integration for time constant switching
GND1	3	ground for 8 V supply
SI	4	signal identification output
INT2	5	integration for signal identification
SSC	6	sandcastle output
50/60 Hz	7	50/60 Hz output
GND2	8	ground for 5 V supply
CS	9	sync output
V <sub>out</sub>	10	V-output buffer
H <sub>out</sub>	11	H-output buffer
V <sub>P2</sub>	12	supply 5 V
CL <sub>out</sub>	13	clock-output buffer
SH	14	start of H-pulse
VCOF	15	current defining VCO frequency
Fi <sub>1</sub>	16	phase detector filtering
Fi <sub>2</sub>	17	phase detector filtering
V <sub>REF</sub>	18	reference voltage
V <sub>P1</sub>	19	supply 8 V
(C)VBS	20	input sync separator



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### FUNCTIONAL DESCRIPTION

(See block diagram Fig.1 and timing Figs 12 to 16)

#### Sync separator

Top-sync and blacklevel are stored and H and V sync pulses are sliced in the middle of both levels (50%).

#### Sync-output buffer

This circuit turns the current pulse from the sync separator into a TTL signal.

#### Sync processing

This circuit assures that phase comparison can operate correctly during V-pulses. Phase jumps initiated by alternating headpulses of VCR recorders are quickly recovered. The sync processing contains the functions H/2 suppression, sync extension and sync interruption.

These three functions are only active if successive pulses have a minimum distance of 1.6  $\mu\text{s}$ .

The H/2 suppression operates with a gate  $-15 \mu\text{s}$  up to  $+14 \mu\text{s}$  around the PHI1-reference and is necessary for suppression of the equalizing pulses. For sync interruption this gate is closed earlier if the detected sync is longer than 4.8  $\mu\text{s}$ .

Only during V-pulses will the duration of the applied pulses be tested. If they are longer than 1.6  $\mu\text{s}$  they will be recognized as sync pulses and enlarged up to 4.6  $\mu\text{s}$ .

#### Phase detector (PHI1)

The phase detector has separate filters for the fast time constant  $T_1$  (pin 17) and normal time constant  $T_2$  (pins 17 and 16). The slow time constant  $T_3$  uses the normal time constant  $T_2$  with reduced control current. For reduction of H-pulse modulation the filter at pin 16 is switched off during sync time if normal time constant  $T_2$  is on. Thus

no frequency shifting of the oscillator is possible during sync.

#### Time-constant switching

This block contains a switch and an impedance converter (buffer). The switch connects the filters at pin 16 and 17 in parallel (normal time constant  $T_2$  or slow time constant  $T_3$ ). The buffer transfers the control voltage at pin 17 to pin 16 (fast time constant  $T_1$ ). Which of the 2 functions is active is determined by the blocks noise detector, V-logic or signal identification.

#### VCO 13.5 MHz

The adjustment of the nominal frequency (13.5 MHz) is achieved at pin 15. The VCO control voltage is applied (from the phase detector) at pin 16.

The control range can be adjusted by the current at pin 18.

Pin 15 can be used to feed in an external frequency. Under these circumstances the internal VCO is switched off by application.

The control voltage at pin 16 can be used to control the external VCO.

#### VCO-buffer

The VCO-buffer delivers a TTL compatible signal of 13.5 MHz to pin 13.

#### ECL-prescaler

This block consists of a :16 asynchronous prescaler.

#### H-divider

This is a divider by 54. It is split into a prescaler :2 and a divider by 27. Out of this block several signals are taken for generation of H-frequently pulses in the H-logic block. These signals must have good timing. This is achieved by special synchronization.

#### H-logic

This block creates all pulses necessary for the SSC generator, the signal identification, the phase detector, the sync preparation and the V-divider.

#### V-divider

The V-divider consists of an asynchronous 10-bit divider and a decoder logic. The divider is clocked with twice the line frequency. The decoder circuit delivers the pulses necessary for the V-logic.

#### V-logic

In the V-logic the V-syncs from the sync separator are evaluated and noise reduced. Also certain operation states are switched ON and OFF. Additionally the reset pulse for the V-divider and the 50/60 Hz information is generated.

#### H-pulse former

The H-pulse starting point can be shifted in this stage, also the gate pulse of  $\sim 2.4 \mu\text{s}$  is generated for use in the digital noise identification block.

#### H-pulse buffer

In this circuit the line signal will be pre-synchronized by output signal of the :16 divider and synchronized by the 13.5 MHz clock. The buffer delivers TTL output signals.

#### V-pulse buffer

The signal out of the V-divider is synchronized with 13.5 MHz clock and converted to a TTL output level.

#### Gap reference

This circuit operates with the gap-principle and is stable with regard to temperature and supply voltage changes.

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### 50/60 Hz output

This is an open-collector output, which is LOW if more than 287 lines/field are detected.

### SSC generator

The SSC generator generates a 3 stage super-sandcastle pulse on an open-collector output, which is able to operate up to 12 volts. The blanking thresholds 2.5 V and 4.5 V are derived from the gap reference (point 16).

### Signal identification with Digital PLL (DPLL)

The analog signal identification with output signal at pin 4 is completed with a DPLL. This PLL is able to lock on the separated sync although the 13.5 MHz VCO is not locked on the input signal. The ratio of the lock condition to the unlock condition influences the voltage at pin 5. The detector circuit of the analog signal identification block evaluates the voltages at pins 2 and 5. If the voltage at pin 5 reaches 4 V (most of the time the PLL is locked) pin 4 will be HIGH. The voltages at pins 2 and 5 together with the state of the V-logic set the operation state of the TDA4691. The TDA4691 is able to accommodate to different input conditions automatically.

Some operation conditions can be set externally by influencing the voltages at pins 2 and 5:

1. Time constant  $T_1$  (fast) on: voltage at pin 2 is limited to 5 V (0 to 5 V).
2. Time constant  $T_3$  (slow) on: voltage at pin 5 is limited to 6.2 V (0 to 6.2 V).
3. Time constant  $T_3$  (slow) inoperative: voltage at pin 2 is limited between 4 V and 6.5 V.
4. Time constant  $T_3$  (slow) inoperative with input signal: voltage at pin 2 is limited to 6.5 V (0 to 6.5 V).
5. VCO frequency fixed to  $f_0$ : pin 2 is set to ground ( $V_2 < 1$  V).

### Noise detector

This block switches the time constant to 'slow' if on standard signal a certain noise level is reached. This noise level is measured in a small window inside the sync pulse.

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>P1</sub>	supply voltage	0	9.0	V
I <sub>P1</sub>	supply current	–	40	mA
V <sub>P2</sub>	supply voltage	0	5.7	V
I <sub>P2</sub>	supply current	–	50	mA
P <sub>tot</sub>	total power dissipation	–	650	mW
T <sub>stg</sub>	storage temperature	–25	+150	°C
T <sub>amb</sub>	operating ambient temperature	0	+70	°C
V <sub>ESD</sub>	ESD-protection on all pins; note 1	300	–	V
I <sub>I/O</sub>	currents on all pins except supply pins 3, 8, 12 and 19	–10	+10	mA
V <sub>I</sub>	voltage applied to pins 1, 2, 4, 5, 7, 14 and 20	0	V <sub>P1</sub>	V
V <sub>I</sub>	voltage applied to pins 9, 10, 11 and 13	0	V <sub>P2</sub>	V
V <sub>6</sub>	voltage applied to pin 6	0	13.2	V
V <sub>15</sub>	voltage applied to pin 15	0	5	V
V <sub>16</sub>	voltage applied to pin 16	0	5	V
V <sub>17</sub>	voltage applied to pin 17	0	5	V
V <sub>18</sub>	voltage applied to pin 18	0	5	V

**Note to the limiting values**

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

**THERMAL RESISTANCE**

SYMBOL	PARAMETER	THERMAL RESISTANCE
R <sub>th j-a</sub>	from junction to ambient in free air SOT146 (without heat spreader) SOT163	65 K/W 85 K/W

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**CHARACTERISTICS**

$V_{P1} = 8\text{ V}$ ;  $V_{P2} = 5\text{ V}$ ; measured at  $T_{\text{amb}} = +25\text{ °C}$ ; unless otherwise specified; application see Figs 10 and 11; video input signal referenced to CCIR standard.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b> (pins 19 and 12; all voltages are measured with regard to ground (pins 3 and 8))						
$V_{19}$	supply voltage		7.2	8.0	8.8	V
$I_{P1}$	supply current		–	20	30	mA
$V_{12}$	supply voltage	same rise time as $V_{19}$	4.5	5.0	5.5	V
$I_{P2}$	supply current		–	15	30	mA
$P_{\text{tot}}$	total power dissipation		–	260	430	mW
<b>Sync separator</b> (pin 20)						
$V_{20(p-p)}$	input voltage (peak-to-peak value)	AC coupled	–	1	2	V
$V_{20(p-p)}$	sync amplitude (peak-to-peak value)		0.1	–	0.6	V
$R_G$	source resistor of generator		–	–	1	k $\Omega$
$I_{20}$	current during sync		–	–30	–	$\mu\text{A}$
$I_{20}$	current during remaining time		–	1	–	$\mu\text{A}$
<b>Black level</b> (pin 1)						
SLH	slicing level H		–	50	–	%
SLV	slicing level V		–	50	–	%
<b>Sync output</b> (pin 9)						
$V_9$	no sync	$I_9 = +1\text{ mA}$	–	0.3	–	V
$V_9$	positive sync	$I_9 = -1\text{ mA}$	2.7	–	$V_{12}$	V
$C_L$	load capacitance		–	–	40	pF
$t_1$	time delay between pin 20 and pin 9	see Fig.3	100	200	500	ns
$t_2$	time delay between pin 20 and pin 9	see Fig.3	100	300	500	ns
<b>Phase detector</b> (pins 16 and 17)						
$f_0$	nominal sync frequency		–	15.625	–	kHz
$f_0'$	$f_{\text{osc}} : 864 = \text{phiref}$		–	15.625	–	kHz
$I_{17}$	current at sync time (fast and normal time constant)		–	$\pm 240$	–	$\mu\text{A}$
$I_{17}$	current at sync time (slow time constant)		–	$\pm 80$	–	$\mu\text{A}$
$I_{16}$	current at sync time	time constant $T_1$	–	$\pm 2$	–	mA
$V_{17}$	filter 2 voltage		1.5	3	4.5	V
$V_{16}$	filter 1 voltage		1.5	3	4.5	V
$\Delta f_0 / \Delta V_{16}$	VCO sensitivity	see VCO	–	360	–	kHz/V
<b>13.5 MHz VCO</b> (pin 15)						
$R_{15}$	$f_0$ defining resistor	see Fig.4(a)	–	3.75	–	k $\Omega$
$V_{15}$	pin voltage ( $V_{19}$ dependent)	see Fig.4(a)	2.9	3	3.1	V
$I_{15}$	current for 13.5 MHz		–720	–800	–880	$\mu\text{A}$
$g_{\text{VCO}}$	transconductance at $f_0$		15.2	–	18.6	kHz/ $\mu\text{A}$



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\Delta f_0/\Delta V_{16}$	VCO sensitivity	4% control range; depending on current at pin 18	–	360	–	kHz/V
<b>Input of external oscillator (pin 15)</b>						
$V_{15}$	pin voltage AC	see Fig.4(b)	1	–	3	V
$V_{15}$	pin voltage DC	dependent on $V_{19}$	–	5	–	V
$R_{int}$	internal resistance	see Fig.4(b)	–	7	–	k $\Omega$
$C_{int}$	internal capacitance	see Fig.4(b)	–	4	–	pF
<b>13.5 MHz buffer (pin 13)</b>						
$V_{13}$	clock HIGH level output voltage	$I_{13} = -1$ mA; $V_{12} = 4.5$ V	2.7	–	$V_{12}$	V
$V_{13}$	clock HIGH level output voltage	$I_{13} = 0$ mA	2.7	–	$V_{12}$	V
$V_{13}$	clock LOW level output voltage	$I_{13} = 2$ mA; $V_{12} = 5.5$ V	0	–	0.8	V
$t_r$	rise time	see Fig.5	–	20	–	ns
$t_f$	fall time	see Fig.5	–	20	–	ns
$D_{13}$	mark-to-space ratio	$V_{13} = 1.5$ V	45/55	–	55/45	%
$C_L$	load capacitance		–	–	40	pF
$\Delta T_{13}$	jitter on clock output (peak-to-peak value)	normal time constant $T_2$ ; measured between lines 25 and 305	–	–	2	ns
<b>H-output buffer (pin 11)</b>						
$V_{11}$	H HIGH level output voltage	$I_{11} = -1$ mA; $V_{12} = 4.5$ V	2.7	–	$V_{12}$	V
$V_{11}$	H HIGH level output voltage	$I_{11} = 0$ mA	2.7	–	$V_{12}$	V
$V_{11}$	H LOW level output voltage	$I_{11} = 2$ mA; $V_{12} = 5.5$ V	0	–	0.8	V
$t_r$	rise time	see Fig.6	–	25	–	ns
$t_f$	fall time	see Fig.6	–	25	–	ns
$t_3$	time relation pin 13 to 11	see Fig.6	–	25	55	ns
$t_4$	time relation pin 13 to 11	see Fig.6	3	–	–	ns
$t_5$	H-pulse width	see Fig.6	3.0	3.6	4.2	$\mu$ s
$C_L$	load capacitance	see Fig.6	–	–	40	pF
<b>Start of H-pulse (pin 14)</b>						
$I_{14}$	current pin 14		–	–	$\pm 100$	$\mu$ A
$t_{61}$	time delay pulse between pin 20 and 11	see Fig.6	–1.1	–1.3	–1.5	$\mu$ s
$t_{62}$	time delay pulse between pin 20 and 11	see Fig.6	–0.6	–0.8	–1.0	$\mu$ s
$t_{63}$	time delay pulse between pin 20 and 11	see Fig.6	3.8	4.0	4.2	$\mu$ s
$t_{64}$	time delay pulse between pin 20 and 11	see Fig.6	5.0	5.2	5.4	$\mu$ s
$V_{14} (t_{61})$	voltage pin 14 (proportional to $V_{19}$ )		0	–	1	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{14} (t_{62})$	voltage pin 14 (proportional to $V_{19}$ )		2	2.4	2.8	V
$V_{14} (t_{63})$	voltage pin 14 (proportional to $V_{19}$ )		3.5	4	4.5	V
$V_{14} (t_{64})$	voltage pin 14 (proportional to $V_{19}$ )		5	5.5	6	V
<b>V-output buffer (pin 10)</b>						
$V_{10}$	V HIGH level output voltage	$I_{10} = -1 \text{ mA};$ $V_{12} = 4.5 \text{ V}$	2.7	–	$V_{12}$	V
$V_{10}$	V HIGH level output voltage	$I_{10} = 0 \text{ mA}$	2.7	–	$V_{12}$	V
$V_{10}$	V LOW level output voltage	$I_{10} = 2 \text{ mA};$ $V_{12} = 5.5 \text{ V}$	0	–	0.8	V
$t_r$	rise time	see Fig.6	–	25	–	ns
$t_f$	fall time	see Fig.6	–	25	–	ns
$t_3$	time relation pin 13 to 10	see Fig.6	–	25	55	ns
$t_4$	time relation pin 13 to 10	see Fig.6	3	–	–	ns
$t_5$	V-pulse width	see Fig.7	280	320	350	$\mu\text{s}$
$t_6$	time delay between pin 20 and pin 10	see Fig.7	12	16	20	$\mu\text{s}$
$C_L$	load capacitance	see Fig.7	–	–	40	pF
<b>Reference (pin 18)</b>						
$V_{REF}$	reference voltage		1.1	1.2	1.3	V
$R_{18}$	control current defining resistor		8	–	30	$\text{k}\Omega$
$\Delta f$	control range VCO		–	$\pm 4$	–	%
$I_{18/1}$	current pin 18 ( $\pm 4\%$ )		–	105	–	$\mu\text{A}$
$\Delta f_a$	adjustable control range		$\pm 3$	–	$\pm 5$	%
$I_{18/3}$	current pin 18 ( $\pm 3\%$ )		–	80	–	$\mu\text{A}$
$I_{18/3}$	current pin 18 ( $\pm 5\%$ )		–	120	–	$\mu\text{A}$
<b>50/60 Hz output (pin 7; open collector; see Fig.8)</b>						
$V_7$	output voltage pin 7; 50 Hz $\geq 287.5$ lines/field = LOW	$I_7 = 1 \text{ mA}$	0	–	0.3	V
		$I_7 = 2 \text{ mA}$	0	0.3	0.8	V
$V_7$	output voltage pin 7; 60 Hz $\leq 287$ lines/field = HIGH		2.7	–	$V_{19}$	V
$I_7$	output leakage current		–	–	50	$\mu\text{A}$
<b>Sandcastle output (pin 6)</b>						
$V_6$	burstkey pulse	see Fig.9	9.5	10	12	V
$V_6$	H-blanking pulse independent from $V_{\text{supply}}$		4.3	4.5	4.7	V
$V_6$	V-blanking pulse independent from $V_{\text{supply}}$		2.3	2.5	2.7	V
$V_6$	voltage pin 6 LOW		0	0.2	0.8	V
$t_w$	pulse width burstkey; 50 Hz	at 6.5 V; see Fig.9	4.0	4.3	4.7	$\mu\text{s}$
$t_w$	pulse width burstkey; 60 Hz	at 6.5 V; see Fig.9	3.3	3.8	4.1	$\mu\text{s}$
$t_2$	time relation between pin 20 and burstkey	see Fig.9	2.2	2.5	2.8	$\mu\text{s}$

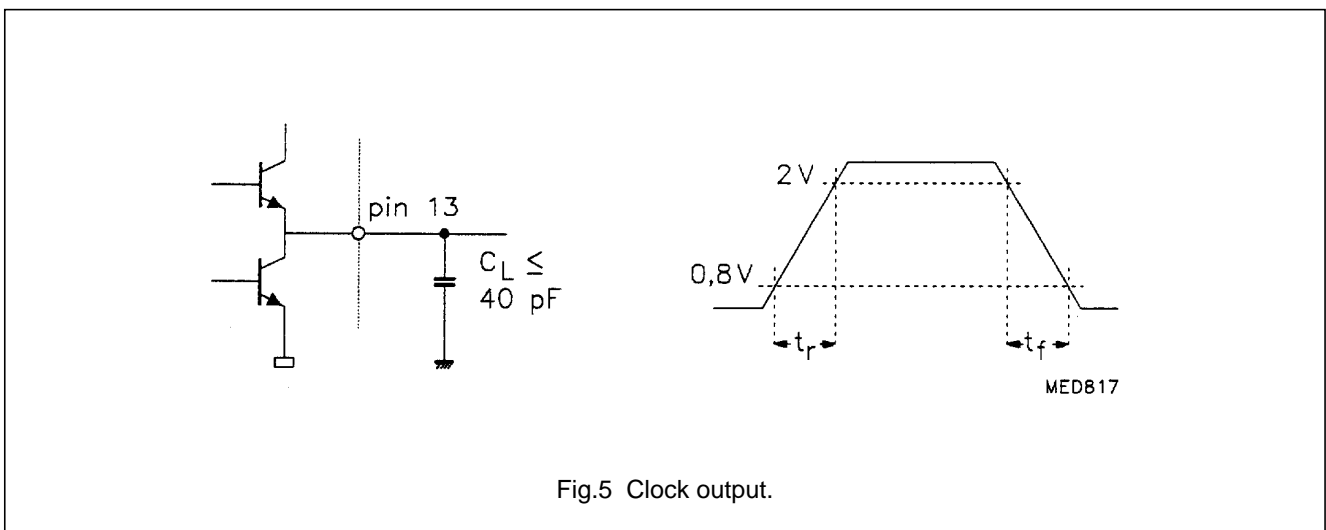
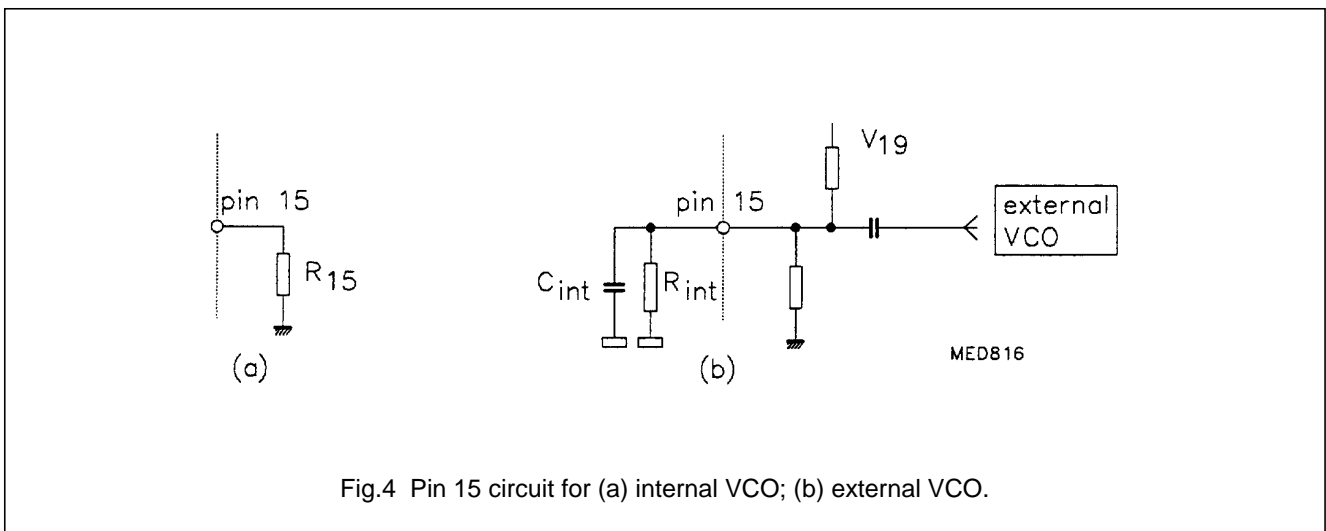
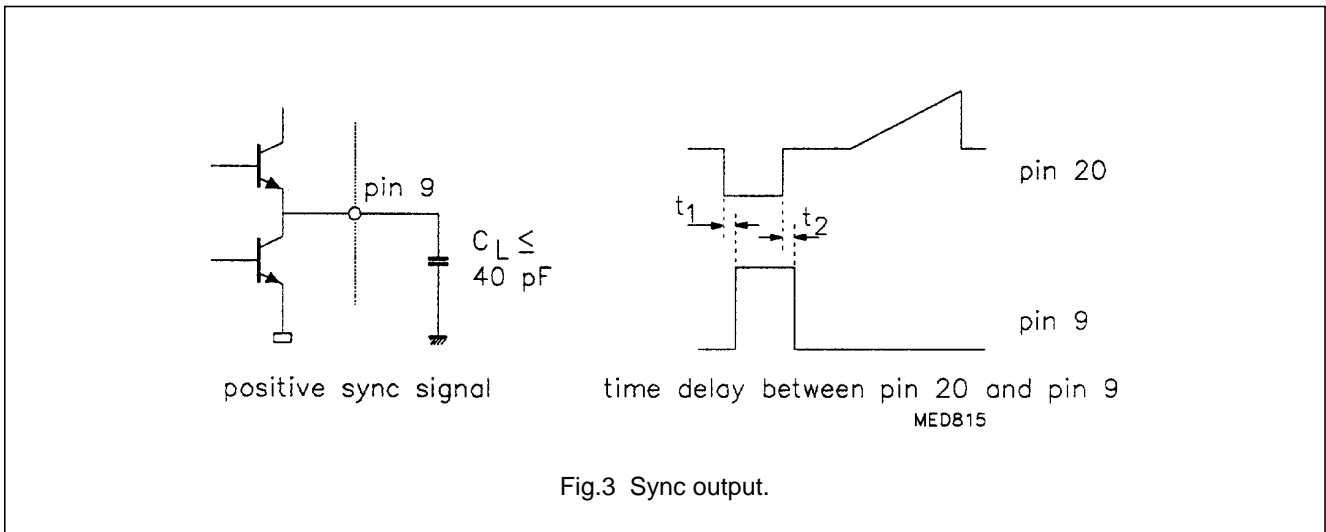
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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t <sub>3</sub>	time relation between pin 20 and blanking	see Fig.9	3.5	4.0	4.5	μs
t <sub>4</sub>	H-blanking time	see Fig.9	–	11.8	–	μs
t <sub>5</sub>	start time H-pulse pin 20 to stop time burstkey pin 6; 50 Hz	H-sync = 4.7 μs; see Fig.9	8.0	9.0	9.7	μs
t <sub>5</sub>	start time H-pulse pin 20 to stop time burstkey pin 6; 60 Hz	see Fig.9	7.5	8.6	9.2	μs
t <sub>6</sub>	V-blanking pulse; 50 Hz		–	–2.5 to +22.5	–	lines
t <sub>6</sub>	V-blanking pulse; 60 Hz		–	–3.0 to +17	–	lines
<b>Integration</b> (pin 5)						
V <sub>5</sub>	no TV signal	see Fig.16	0	–	2	V
	TV signal	see Fig.16	4	–	–	V
V <sub>5</sub>	slow time constant on		5	–	6.2	V
<b>Signal identification</b> (pin 4; open collector via R <sub>4</sub> to V <sub>19</sub> or V <sub>12</sub> )						
V <sub>4</sub>	voltage pin 4, if no signal is identified	I <sub>4</sub> = 1 mA	0	–	0.3	V
		I <sub>4</sub> = 5 mA	0	0.2	0.8	V
V <sub>4</sub>	voltage pin 4, if signal is identified		–	–	V <sub>19</sub>	V
I <sub>4</sub>	leakage current		–	–	50	μA
<b>Integration</b> (pin 2; see Fig.15)						
V <sub>2</sub>	no signal at pin 20		–	1.5	–	V
V <sub>2</sub>	noise at input pin 20		–	3	–	V
V <sub>2</sub>	switching T <sub>3</sub> to T <sub>1</sub> (delay 7 fields)		–	2.5	–	V
V <sub>2</sub>	switching T <sub>3</sub> to T <sub>1</sub> (noise and signal at input pin 20)		–	2.5	–	V
V <sub>2</sub>	release V-divider		–	4	–	V
	hysteresis		–	–0.2	–	V
V <sub>2</sub>	release time constant normal (T <sub>2</sub> ) signal identification at pin 4		–	5	–	V
	hysteresis		–	–0.2	–	V
V <sub>2</sub>	release noise detector		–	6.5	–	V

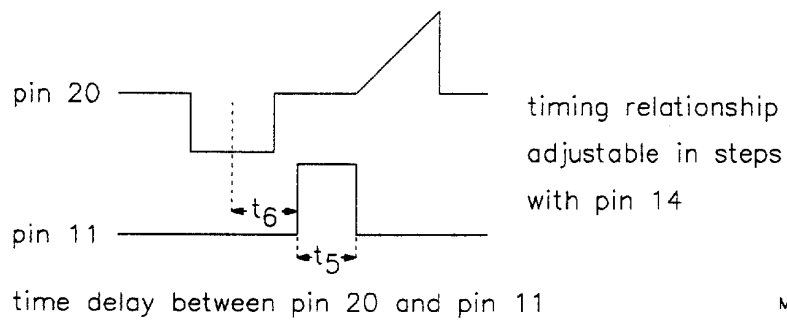
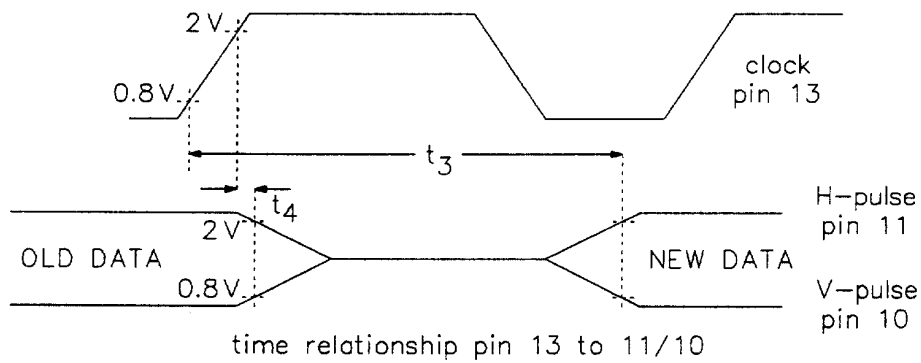
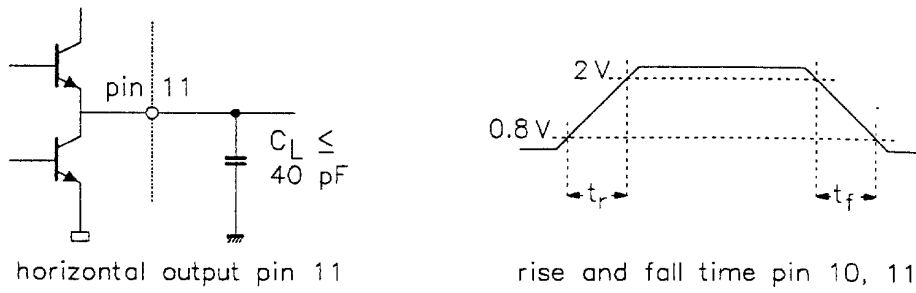
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Fig.6 Time relationship of pin 10/11 to pin 13/20.

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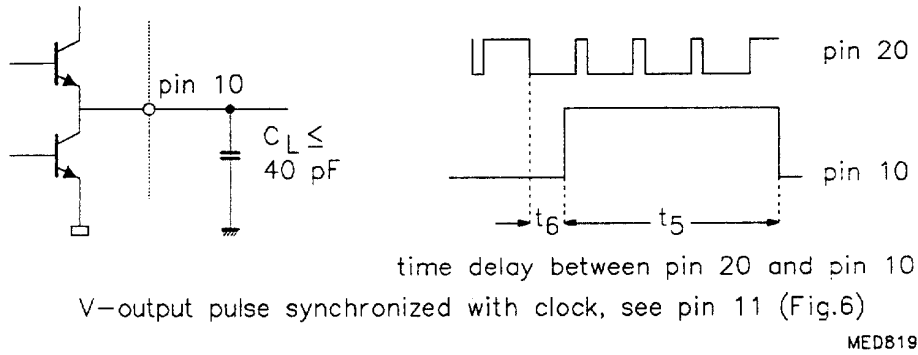


Fig.7 Time relationship pin 10 to pin 20.

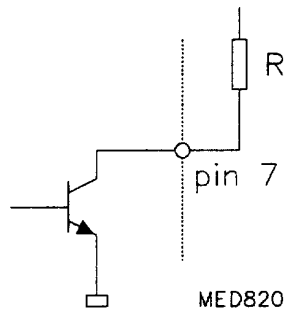


Fig.8 50/60 Hz output.

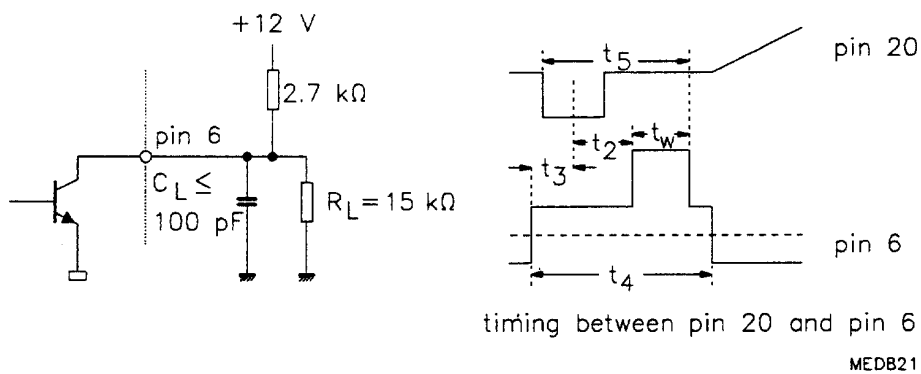
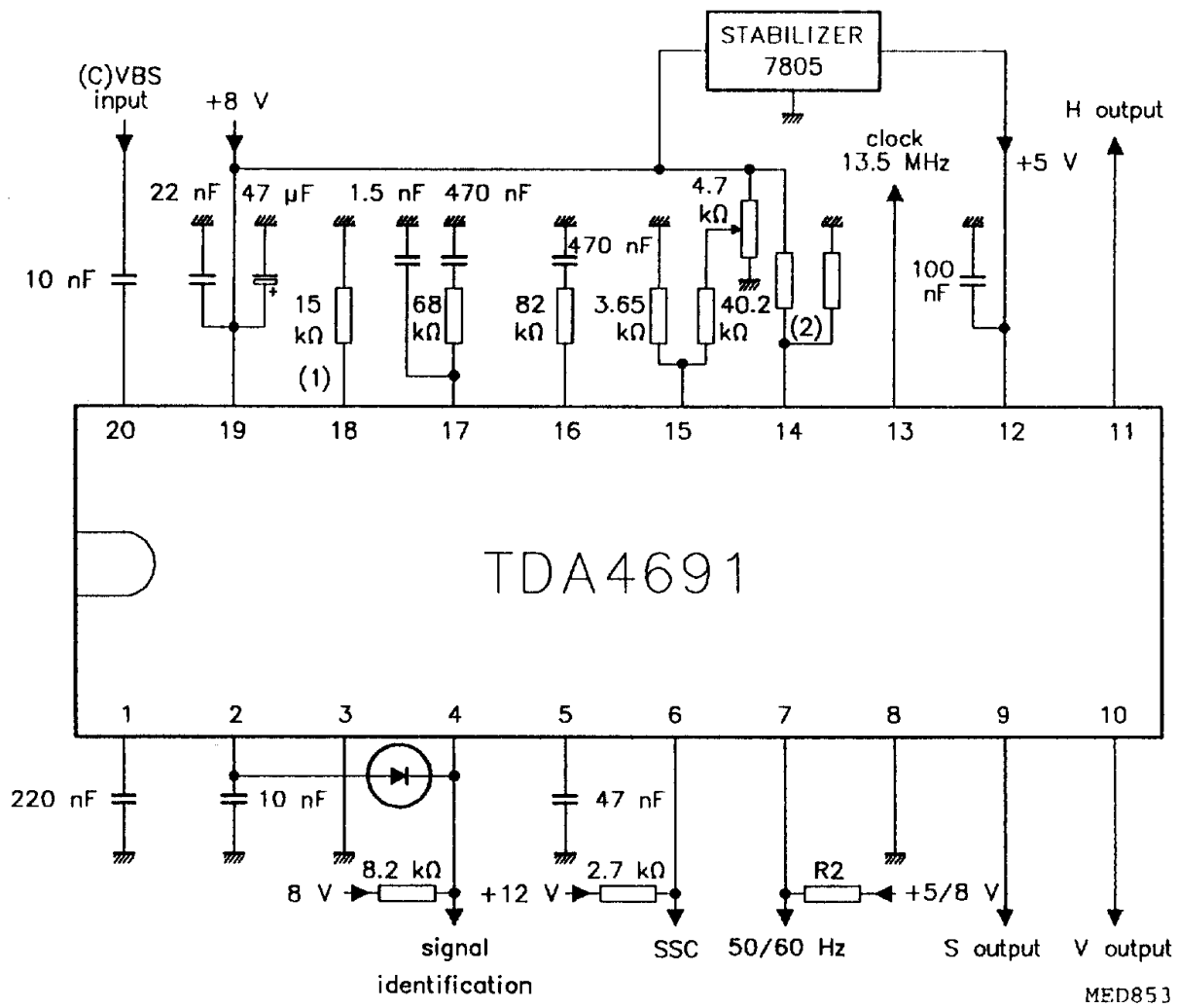


Fig.9 Sandcastle output.

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- (1) control range VCO 4%; see CHARACTERISTICS.
- (2) depending on H output shift; see CHARACTERISTICS.

V <sub>P</sub> (V)	R2 (kΩ)
5	5.1
8	8.2

Fig.10 Application diagram.

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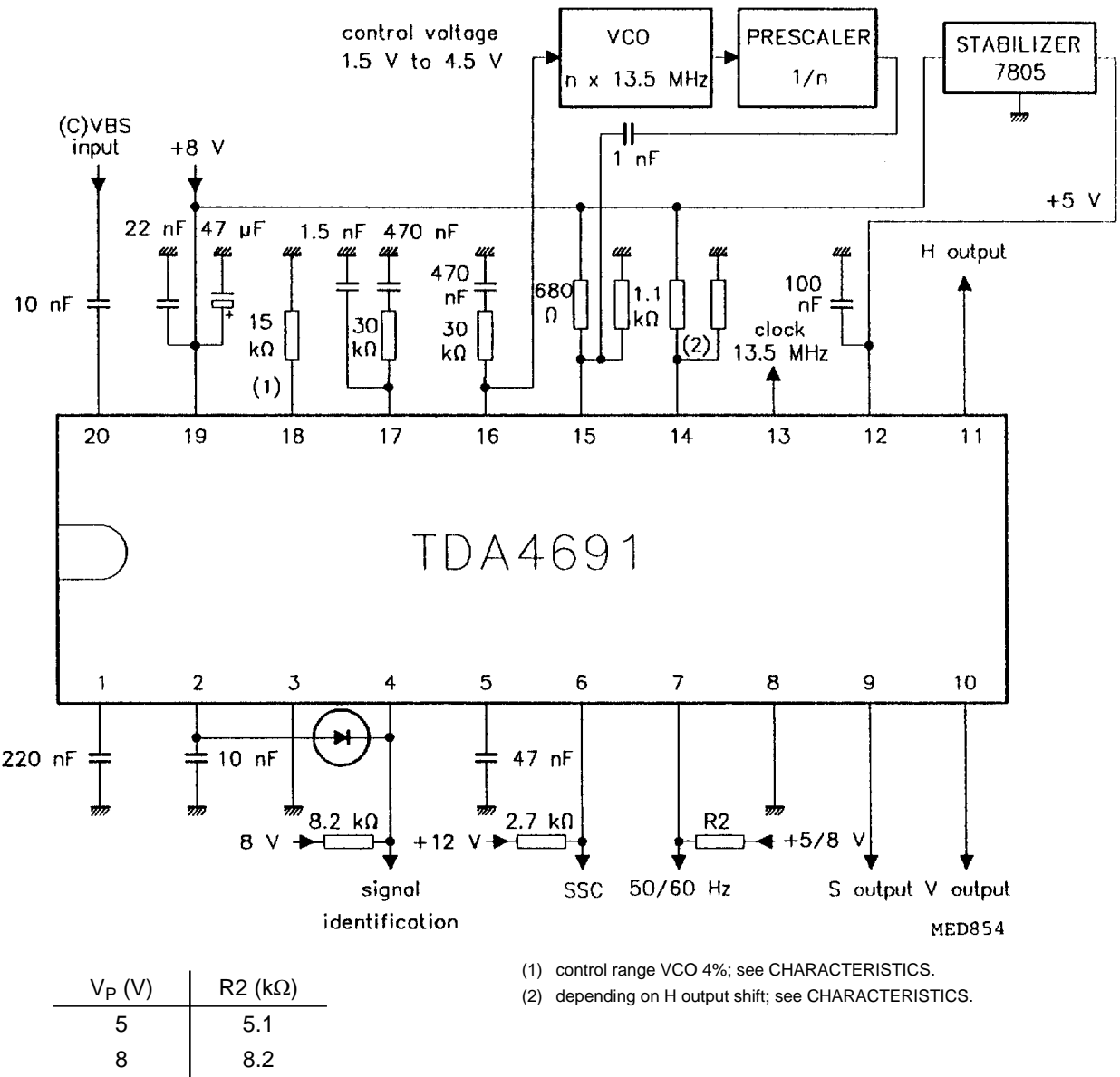


Fig.11 TDA4691 with external VCO and prescaler.



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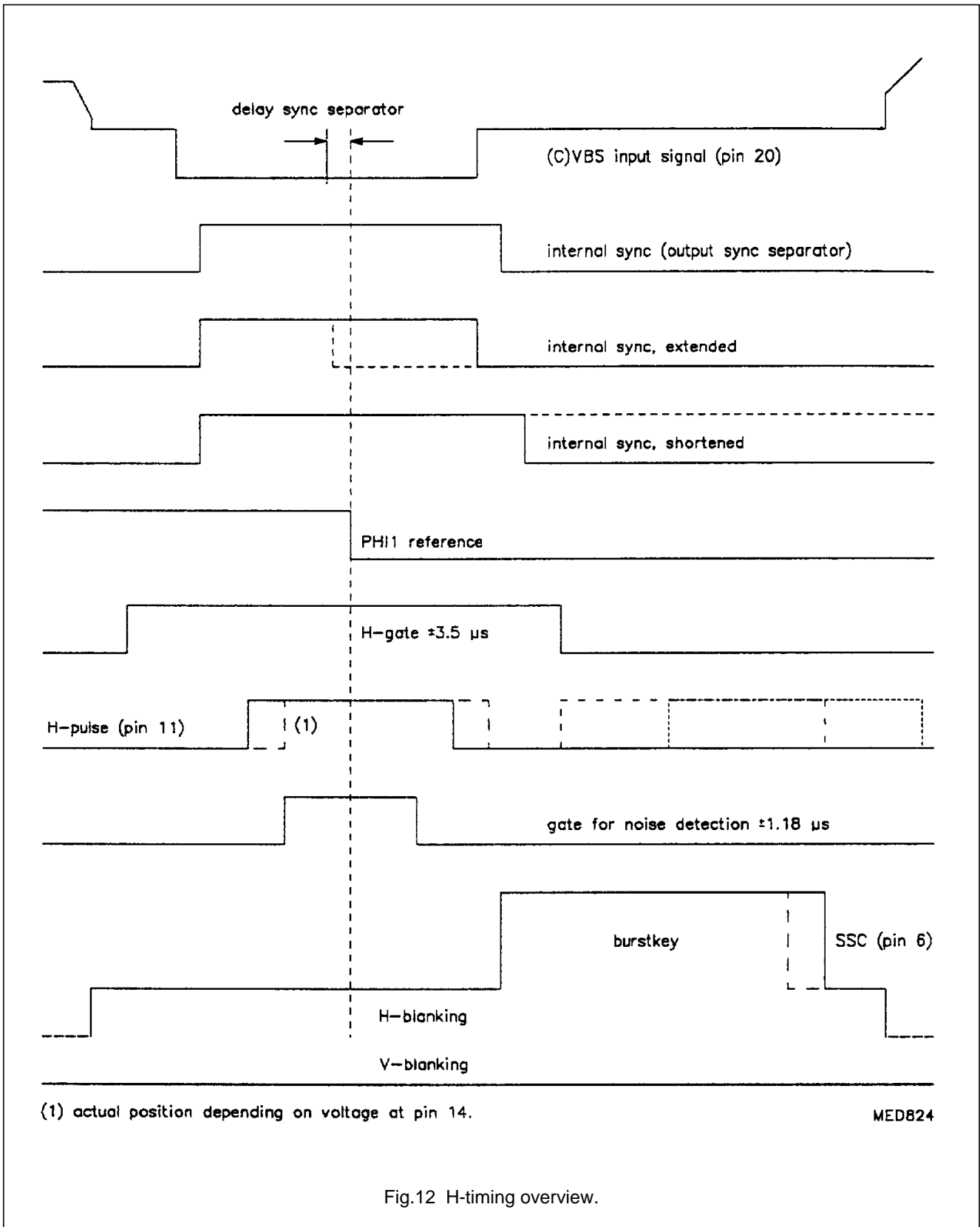


Fig.12 H-timing overview.

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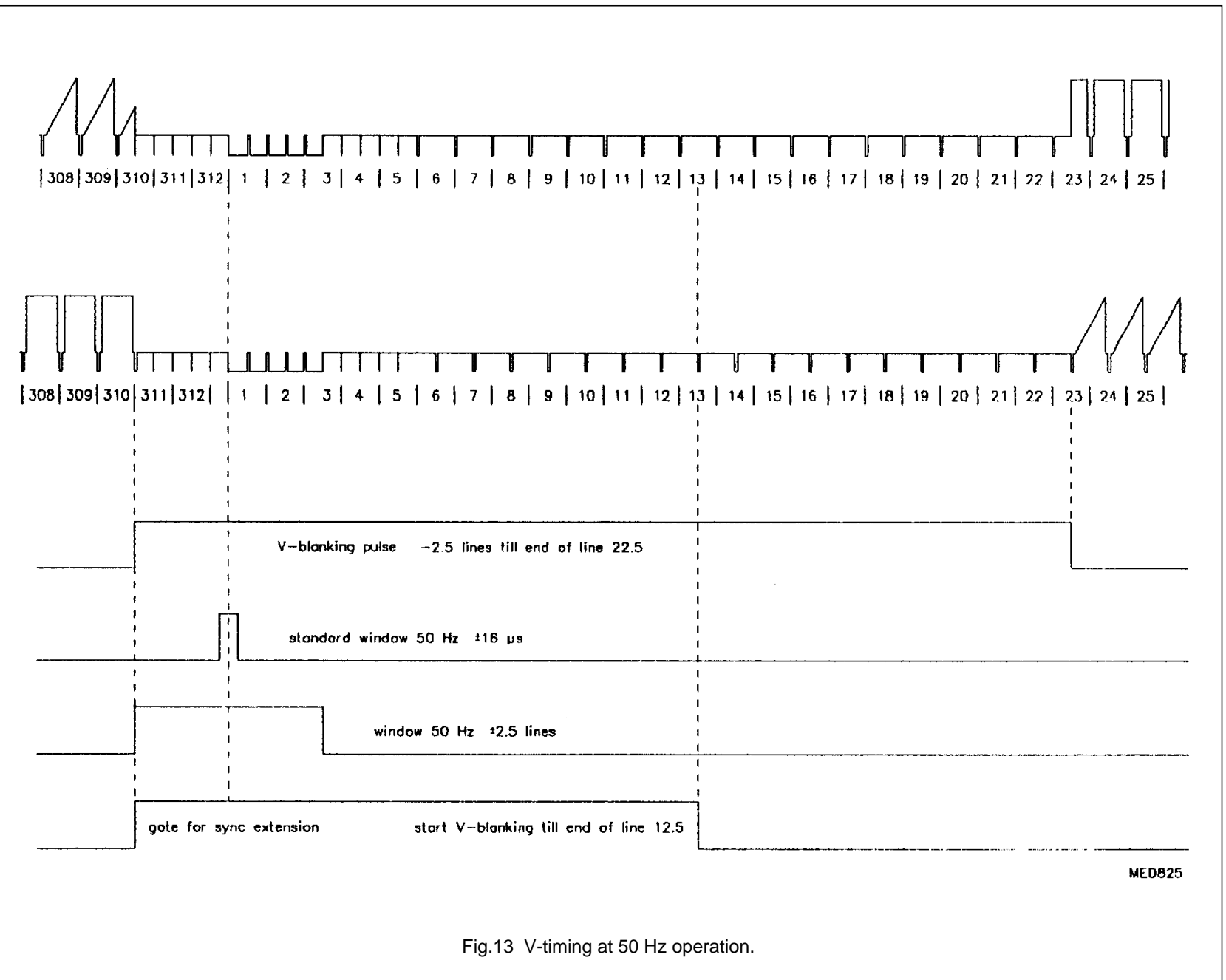
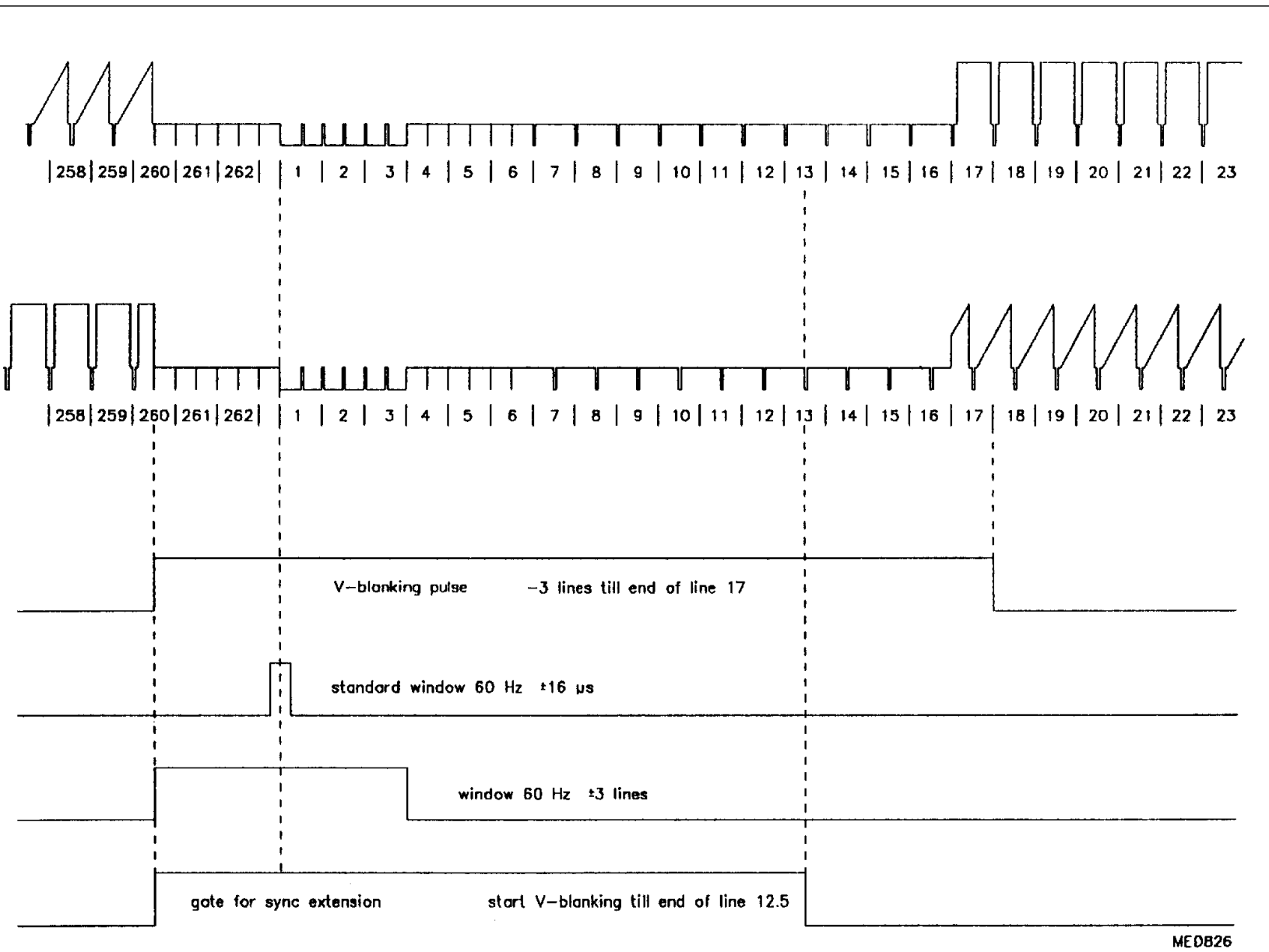


Fig.13 V-timing at 50 Hz operation.

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Fig.14 V-timing at 60 Hz operation.

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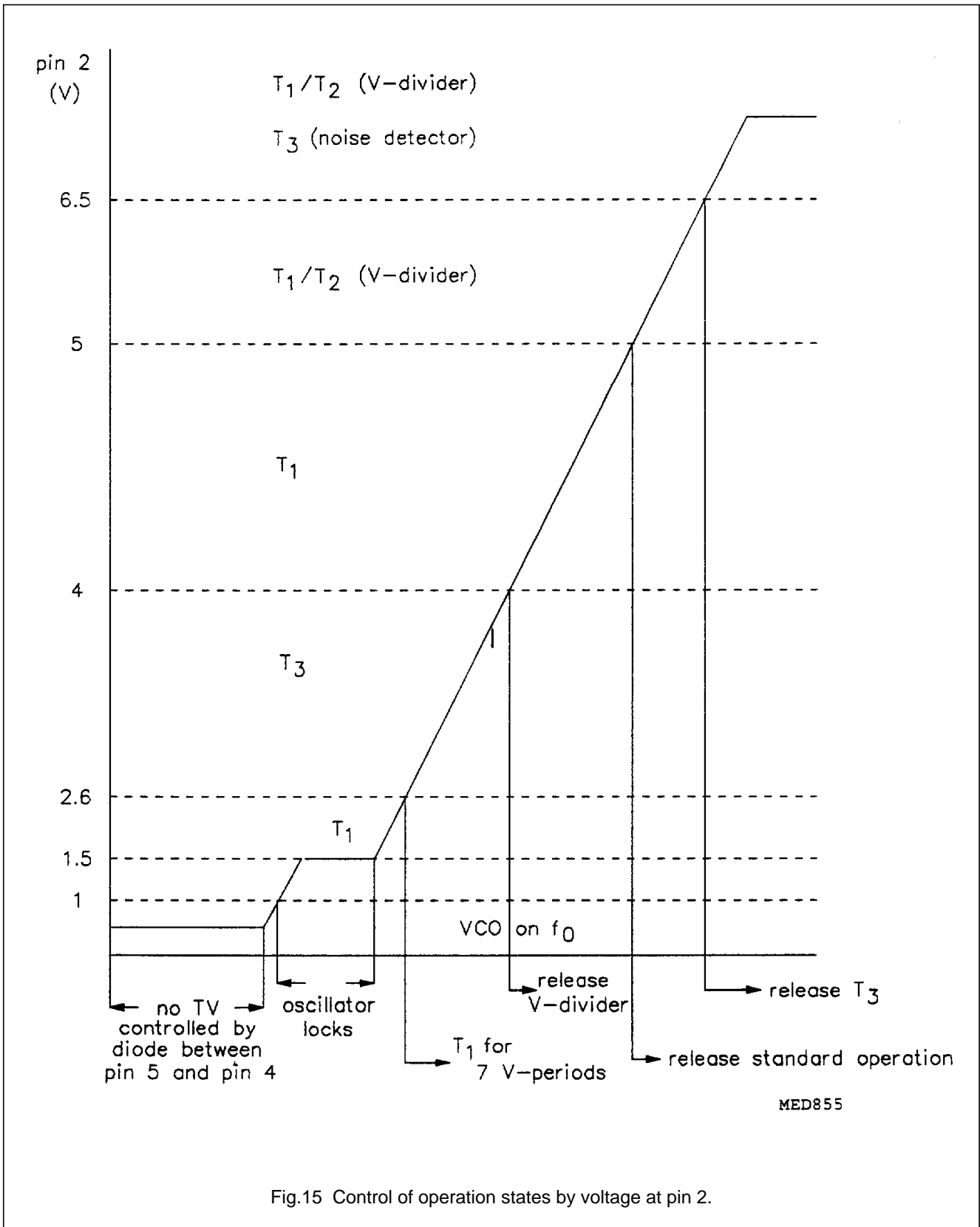
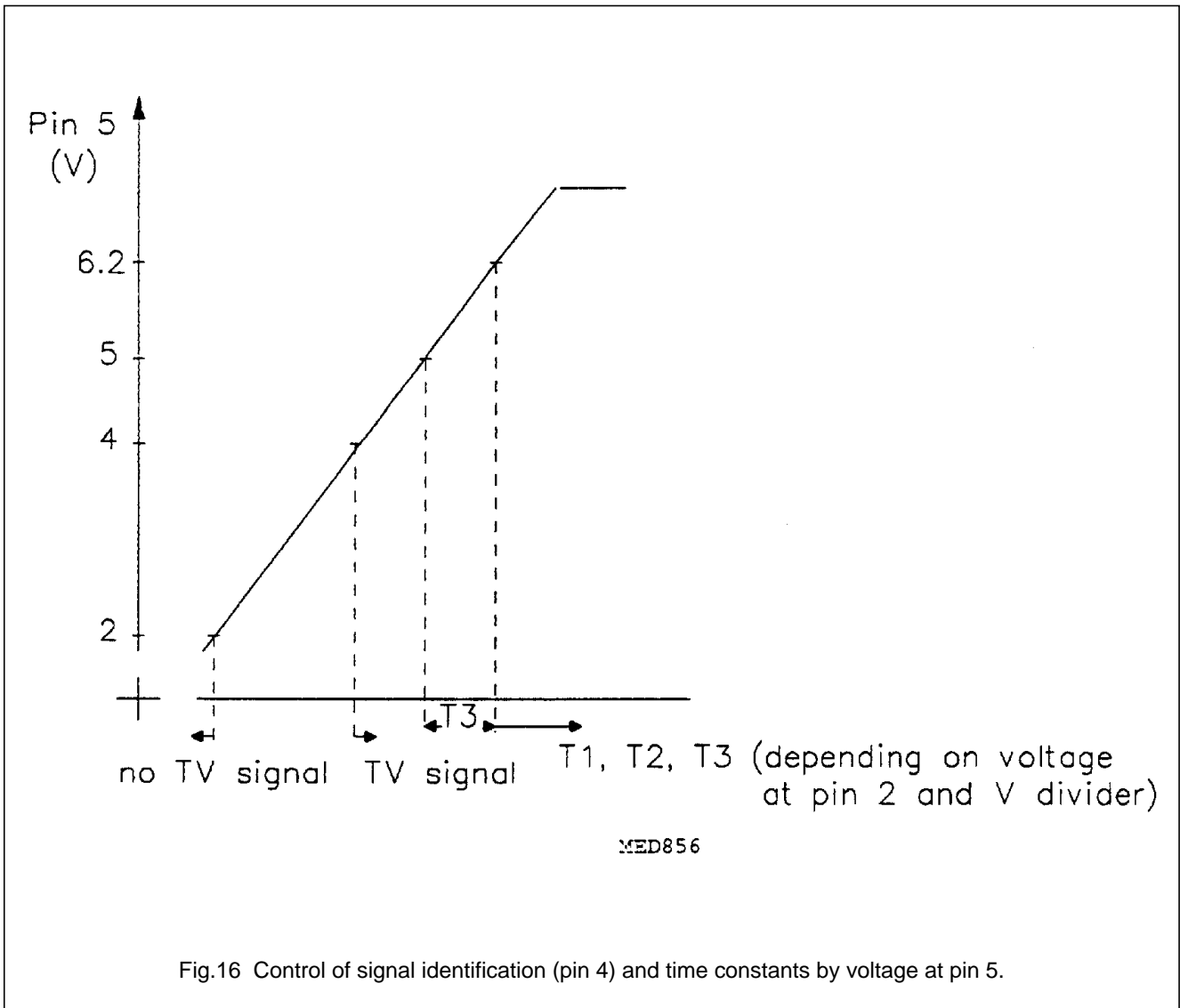


Fig.15 Control of operation states by voltage at pin 2.

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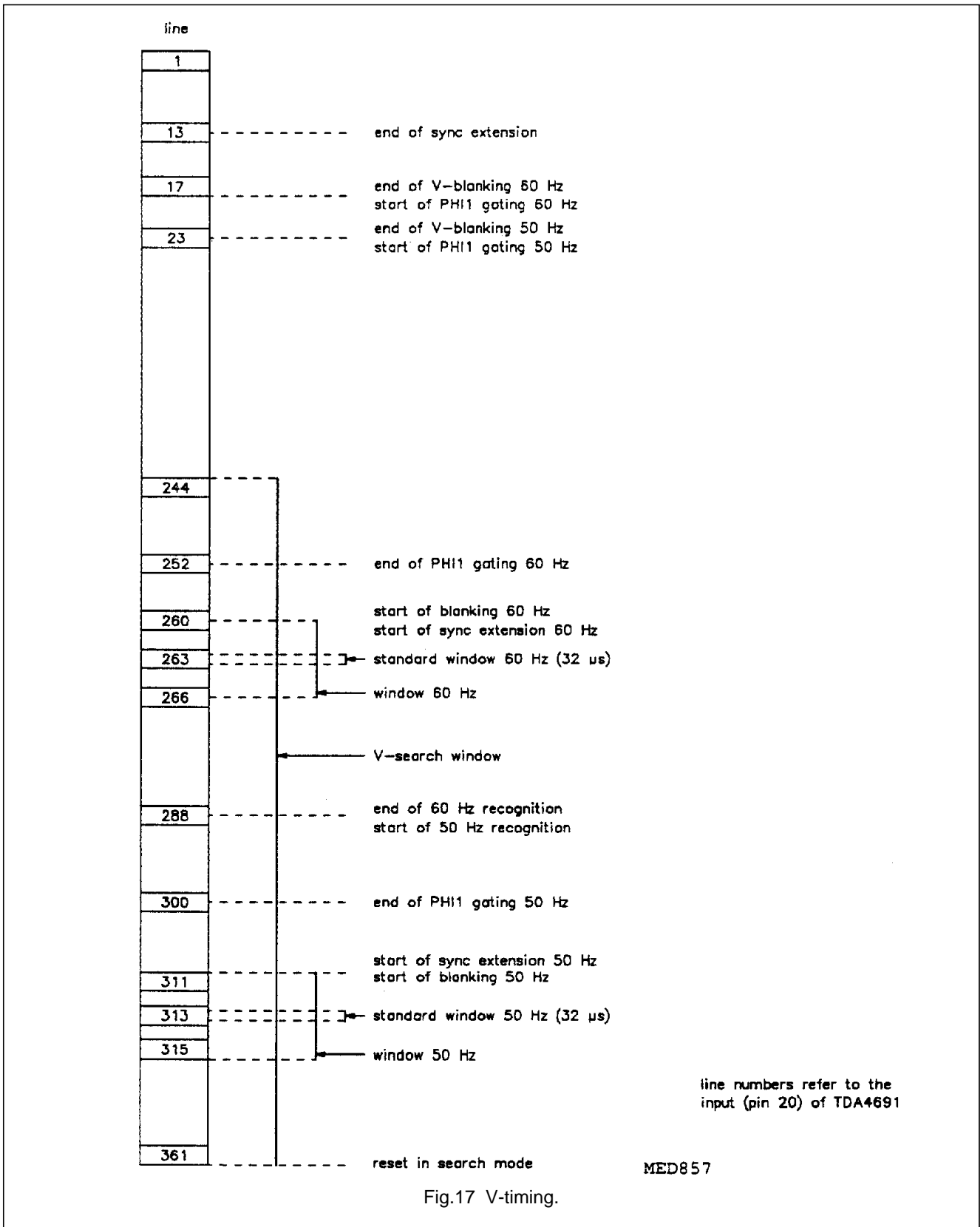


Fig.17 V-timing.

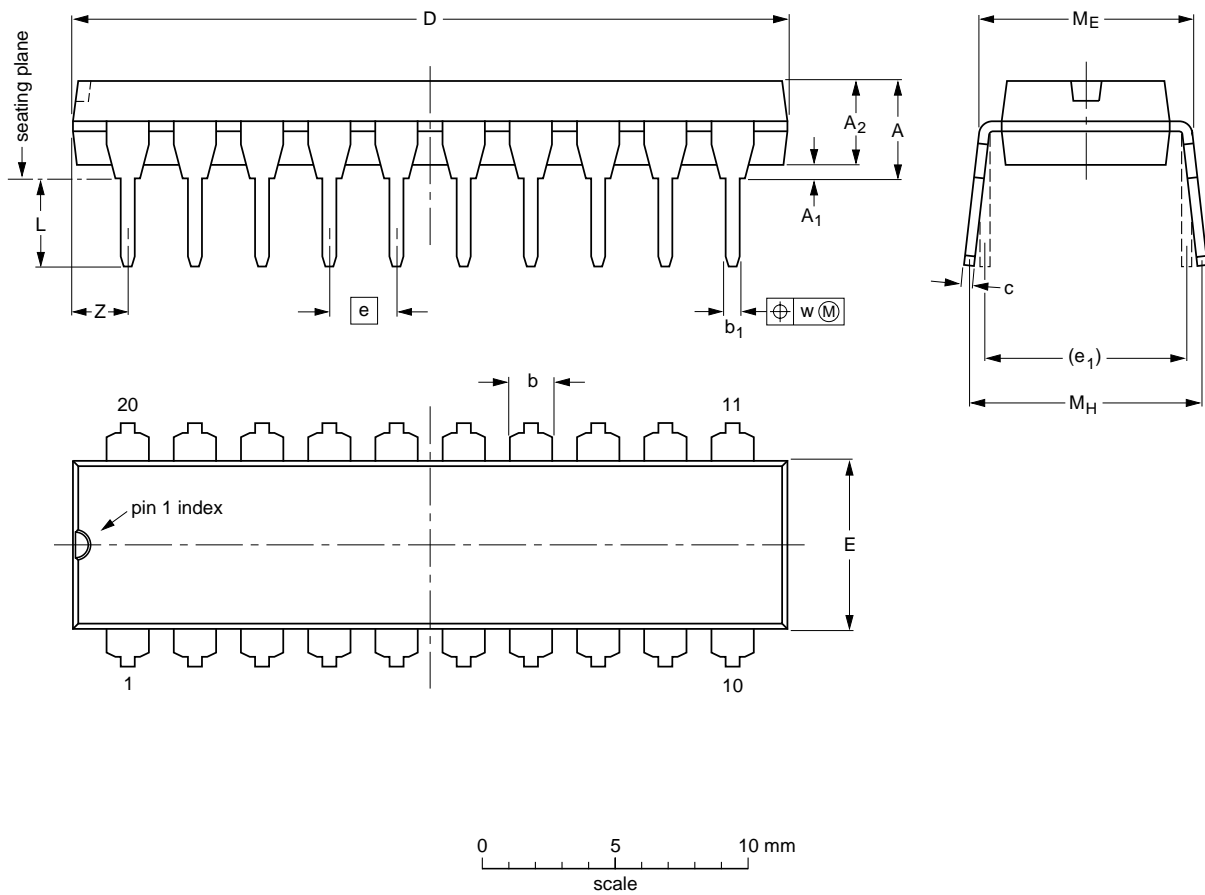
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PACKAGE OUTLINES

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

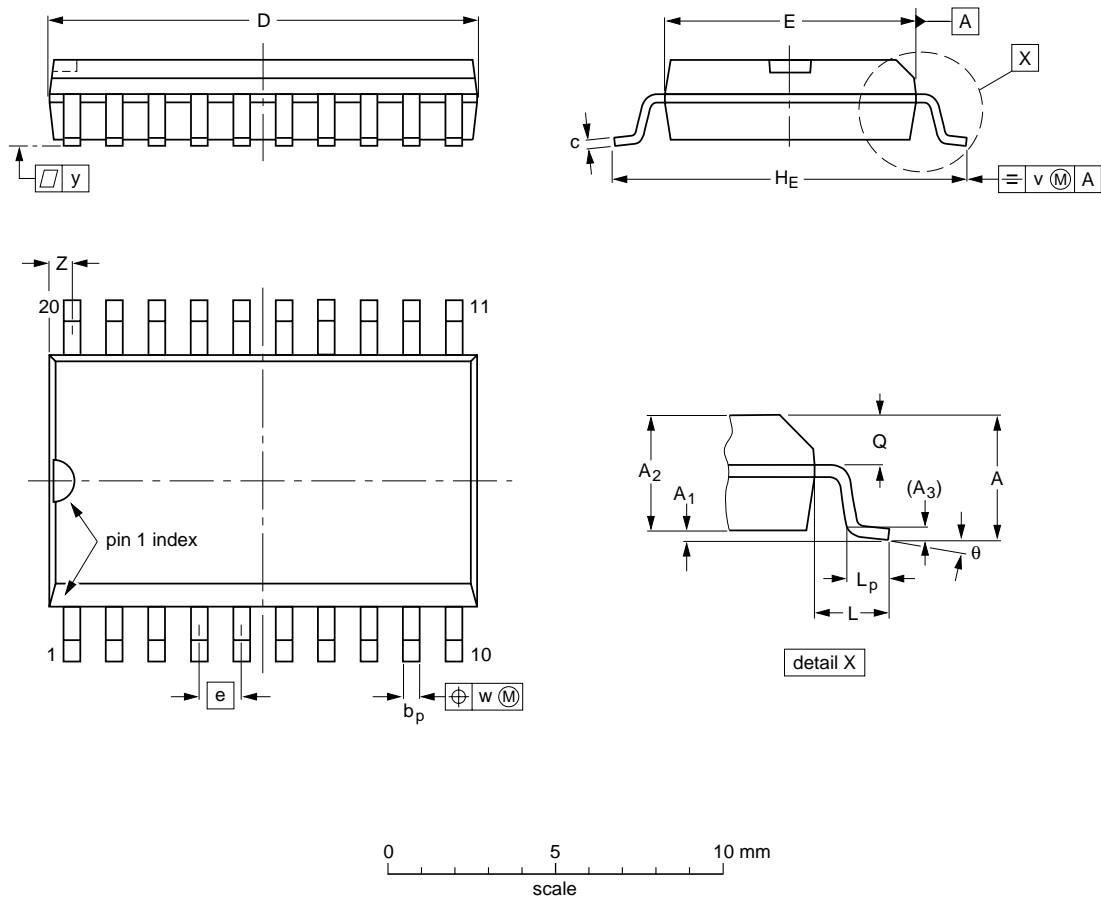
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22



## Sync Processor with Clock (SPC)

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### DIP

##### SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### SO

##### REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

##### WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## Sync Processor with Clock (SPC)

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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